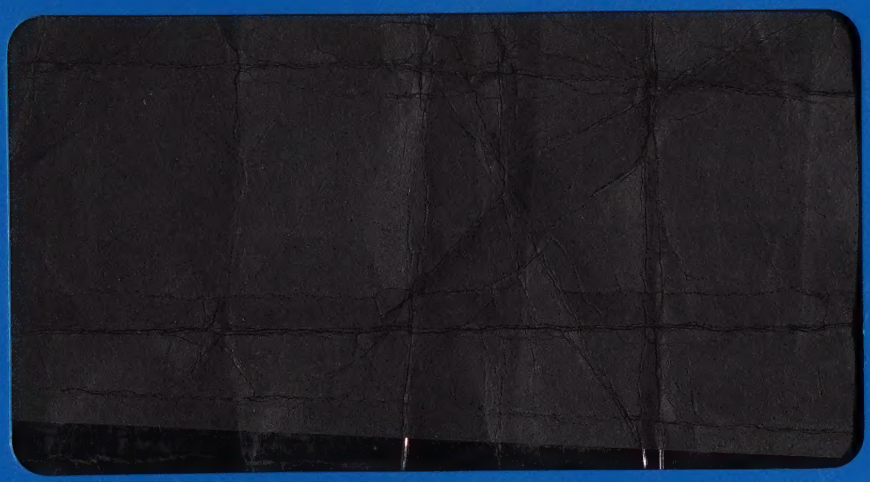

Scientific
Atlanta

Spectral Dynamics Division

SERIAL _____

SERVICE MANUAL

SD375
Dynamic Analyzer II

(Volume 1)

619 679-6000

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Appendix

A SERVICE MANUAL TV-50 DATA DISPLAY MONITOR

B SD375 WIRE STRING LIST

C TYPE N30002 CENTRAL PROCESSING ELEMENT (CPE)

D TYPE SN74S482N ADDRESS GENERATOR

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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

The SD375 Dynamic Analyzer II is a stand-alone real-time spectrum analyzer featuring a raster-scan crt, touch-tone operated controls, dual channel analysis, and alpha-numeric readout of displayed signal parameters. More detailed information about SD375 features is contained in later paragraphs.

There are two volumes (Volumes I and II) which comprise the SD375 service instructions. This section contains references to other documents that may be helpful to maintenance personnel and a brief description of the instrument; its capabilities, options, and specifications.

The detailed theory of operation of the Dynamic Analyzer II is contained in Section II. The calibration and alignment procedures are contained in Section III. Parts replacement data is contained in Section IV. Section V provides detailed theory of the Dynamic Analyzer II options.

The appendices of Volume I contain information on the Data Display Monitor (TV50) raster-scan crt, and the wiring interconnection table (string list). Information about several hardware devices are included in the appendices to facilitate an understanding of the theory of operation contained in Section II.

Volume II is composed of detailed schematic and printed wiring assembly drawings.

This manual is written for technicians who are experienced in analog and digital circuitry. Section II should be read and understood before attempting to troubleshoot or calibrate the instrument.

1.2 OTHER DOCUMENTATION

The User's Manual is shipped with each instrument. Reference should be made to that document when instructions for unpacking, initial checkout and repacking for shipment are required. Copies of available manuals for the SD375 may be obtained by ordering the following manual titles:

SD375 User's Manual
SD375 Service Manual
SD375 User's Manual Translator Option
SD375 User's Manual 1/1 & 1/3 Octave Option
SD375 Instruction Manual Digital I/O Interface Option

Technical papers are available from Scientific-Atlanta which provide user oriented background information. For a list of this material, contact either your local sales/service office or the San Diego Group. The following applications manuals are also available:

Title	Number
Dynamic Analyzer Applications	SD101B Appl.
Linear/Log Sweep Oscillator Applications	SD104B Appl.
Signal Analysis Using Digital Techniques	DSP004
Trigonometric Transforms	DSP005
What is "Dither"	RTA-1
Noise Source Analysis	SDRC-1

1.3 EQUIPMENT DESCRIPTION

The Model SD375 Dynamic Analyzer II is a stand-alone, hard wired, dual channel instrument that combines a 400-line per channel spectrum analyzer, digital signal processing, ensemble averaging, and a dual-trace raster scan crt in a single portable unit. Specific features and functions are contained in paragraph 1.9.

The instrument is a microprocessor-based FFT analyzer and signal processor that analyzes frequencies up to 100 kHz with 400-line per channel resolution.

Spectral data is displayed on the crt. Harmonic relationships (orders) between signal components can be directly displayed and any 25% of the display can be expanded to the full width of the crt for detailed examination. An alphanumeric readout on the crt, in conjunction with a cursor and the crt display grid, provides information in a variety of engineering units (e.g., mil/sec, mil displacement, and g). Automatically-scaled X-Y recorder outputs and X-Y display outputs are also provided.

The capability of performing Structural Transfer Functions adapts the SD375 to almost any application in design, production testing, and maintenance troubleshooting of rotating machinery. Direct read out of sound pressure levels makes it useful in a broad variety of acoustic studies.

Some of many applications for the SD375 are:

- Noise and vibration studies of vehicles and farm/construction equipment
- Engineering instruction in vibration and signal analysis
- Drive-by and fly-by tests of new vehicles and aircraft
- Analysis of underwater sounds and sonar signals
- Modal analysis of automotive engines, frames and bodies
- Vibration analysis of gas and steam turbines to define failure mechanisms
- Medical and biological stimulus vs. reaction studies

- Structural-integrity and tool-chatter investigations of machine tools
- Aircraft flutter and vibration analysis
- Dynamic stress analysis of heavy off-highway equipment
- Railway equipment noise-reduction programs
- Household appliance development studies
- Computer disc-drive design

1.4 STANDARD FEATURES (CHARACTERISTICS)

The following are some of the standard features that are provided in the SD375. The complete list of features can be found in the specifications section (paragraph 1.9) of this manual:

Front-panel selection of twenty-one frequency ranges in a 1, 2, 4 and 5 sequence from 1 Hz to 100 kHz full scale.

A built-in dual-trace raster scan crt with cursor-controlled X2 and X4 magnification for expanding any selected portion of the X-axis spectrum for full screen viewing.

A display grid which is internally generated by the microprogram and projected on the crt to correspond with selected front-panel functions.

A built-in averager for signal-to-noise enhancement in the frequency or time domain. The number of averages can be specified by the number of ensembles (N) or total averaging time (T) to the nearest second. The averaging number is entered through the keyboard and can be *any* integer number. The averaged display is normalized after each average for spectrum, transfer function or correlation displays. Averaging in the EXPO mode is performed linearly up to the selected number of averages and then continues exponentially, with a selected time constant, until terminated by the operator.

A peak hold mode, which detects and retains the highest level in each of the 400 displayed cell locations. The peak values can be stored or erased by the operator.

An alphanumeric readout on the raster scan crt gives a readout of the following parameters for any point on the spectrum display:

a. Frequency in Hz

b. Frequency in KCPM

c. Harmonic order number relative to any selected fundamental

d. Amplitude Volts (rms)

e. Amplitude dB

f. Amplitude in EU

g. ΔX

h. Overall level in Vrms, dB and EU

i. ΔP

j. PSD (EU^2/Hz)

k. FWD Transform — CH A

l. FWD Transform — CH B

NOTE

Transducer sensitivity, dB REF and threshold percentage for transient capture are entered by means of a front-panel keyboard for direct engineering unit, relative dB readings or to capture transients exceeding a set threshold level in a positive or negative direction.

A cursor that combines an intensified dot and a vertical line for locating specific spectral components.

A harmonic cursor mode with fine tuning which intensifies all integer orders of the selected fundamental components.

A SIMULPLOT feature which enables continuous viewing of the complete spectrum while plotting, plus:

a. Selectable Plot Rate. Four different plotter rates, (15 sec, 30 sec, 45 sec and 60 sec per plot) can be selected through the keyboard.

b. Interface to Analog X-Y plotters with pen lift.

c. Plot time waveform.

d. Log-X sweep rates.

e. Offset and Gain control for upper trace.

f. Plot expanded display.

A remote feature that provides the following lines for remote control OR'ed with front-panel control:

a. START/STOP AVG

b. Erase

c. 1

d. TRANS ARM

e. MEMORY Hold/Update

f. TRANSFER M1 → M2

g. TRANS AUTO

1.5 SD375 OPTIONS

NOTE

The SD375 is configured to easily add these standard options initially or later as your signal processing and analysis requirements dictate. Front panel controls and main frame accommodations for the options are built into every analyzer.

1.5.1 Digital Translator (-1 Option)

The -1 option provides six zoom (i.e., frequency magnification) factors — 2, 5, 10, 20, 50 and 100 for each analysis range. A zoom factor of 100, for example, increases the frequency resolution by 100 times the normal baseband resolution and, at the same time, improves the signal-to-noise ratio of the measurement. The factor best suited to the analysis task at hand can be instantly selected on the front panel for separating closely spaced frequency components.

When the translator (XLTR) is turned on, the center position of the zoom window is automatically established by the cursor location. If the cursor is moved, the window is automatically relocated within the selected full-scale analysis range. The cursor always indicates the window's center frequency while the lower and upper window edge frequencies are annotated at the left and right ends of the X-axis grid as shown in the figures at the left.

The CF SET control locks the window position and enables the cursor to be moved to any point within the window for high resolution frequency readout. The ΔP cursor feature can be used to read the RMS level of the signal within the zoom window.

Translator gain of 1, 2, 4 or 8 recovers the dynamic range lost when zooming in with a narrow window on a portion of a broadband spectrum. This gain is inserted prior to spectrum analysis of the windowed signal and permits detection of signal amplitudes more than 80 dB down from full scale.

1.5.2 1/3 and 1/1 Octave Analysis (-2 Option)

Adding the -2 option to the SD375 combines 1/3 octave, 1/1 octave, and dual channel narrowband analysis capabilities into one instrument. Selection of the 1/3 or 1/1 octave display mode is provided from a menu through the LIST front panel control.

The -2 utilizes a *single pass parallel process* data acquisition method for synthesizing 1/3 and 1/1 octave spectra. It offers three distinctive advantages over serial multiple-pass techniques . . .

First, the entire 1/3 or 1/1 octave spectrum is synthesized from the same segment of the data record, thus always assuring a valid spectrum.

Second, dual input buffer storage enables 1/3 or 1/1 octave processing of continuous impulsive signals.

Third, analysis time is reduced by utilizing overlap processing techniques on the lower frequency data group.

Thirty full 1/3 octave and ten full 1/1 octave bands of data plus the overall RMS level are displayed on each 1/3 and 1/1 octave full scale analysis range. Data signals can be processed independently on CH A or CH B and the 1/3 octave spectrum stored in their respective averager memory locations. Post data manipulation (+, −, ÷), selected through the menu, can be performed on stored A and B 1/3 octave spectra.

1.5.3 Digital I/O (-3xxx Option)

With the -3xxx options the SD375 can provide IEEE-488 and RS-232 interface for complete remote front-panel control and convenient output of digital data. Therefore, due to the various peripheral interface and computer data output formats available, the -3 option uses a four digit option designator. For further information, concerning this option and or designations available, contact the nearest Scientific-Atlanta office or representative.

1.5.4 Synchronous Signal Generator (-4 Option)

This convenient signal source provides broadband white noise, band limited pseudo-random noise and single sinewave analog outputs for excitation of systems or networks for performance evaluation. The signal generator output mode is established from a PRGM menu and its output amplitude selectable from 0.05V to 10V in a 1, 2, 5 sequence.

The pseudo-random noise is synced to the internal ADC clock and its sequence length matches the memory period of the analyzer. A trigger output, coincident with the start of each sequence, is provided. In zoom mode, the pseudo-random frequency output is concentrated within the zoom window.

1.6 SPECIFICATIONS

1.6.1 Inputs

Impedance:	100k ohms
Coupling:	DC, AC (−3 dB at 0.5 Hz), AC only on 10, 20, and 50 mV input ranges.
Range:	11 input level ranges are available, from 0.01 Vrms to 20 Vrms, in a 1, 2 and 5 sequence. The 0.01, 0.02, and 0.05 Vrms ranges are not available when using the 100 kHz analysis frequency range. Level ranges may be selected either manually or automatically.
Max Input:	50 Vrms
A/D Converter:	12 Bits

Digital Input:	16 bit digital input to each input memory through optional digital I/O.
Anti-Aliasing Filters:	Automatically selected on each channel for each frequency range with initial 120 dB/octave rolloff for 70 dB rejection of aliasing terms; 1, 2, 4, and 5 Hz frequency ranges utilize the 10 Hz lowpass anti-aliasing filter. Amplitude Match: ±0.3 dB Phase Match: 10 Hz to 5 kHz ±1° 10 kHz to 50 kHz ±3° 100 kHz ±5°
Sampling Rate:	2.56 × full scale frequency range selected on internal sampling control. External sampling control provided.
Sync Reference:	Accepts TTL level input as trigger reference for dual-channel time domain signal averaging or synchronous spectrum functions.
Overload:	Front panel LED indication on each channel.
Level Indication:	0.1 and 0.5 F.S. LED's on each channel.
Data Editing:	Rotate contents of input memory for CH A or CH B. Zero selected parts of input memory for CH A or CH B.
Auto Trigger:	Synchronizes data loading of input memories at keyboard selected threshold level.
Test Signal:	Replaces input signal with internally generated periodic signal.

1.6.2 Analysis

Resolution:	400 lines of real time or averaged spectrum information on each analysis range. Each channel processes a 1024 point transform.
Frequency Ranges:	21 total ranges from 1 Hz full scale to 100 kHz full scale in 1-2-4-5 sequence.
Real Time Frequency:	4 kHz for single-channel forward tranform. 2 kHz for dual-channel forward transform. (Through to output display).
Frequency Response:	±0.5 dB at filter centers over entire frequency range up to 30 kHz. ±1.0 dB at filter centers from 50 kHz to 100 kHz.
Frequency Accuracy:	±0.0025
Dynamic Range:	70 dB with averaging from full scale to minimum discernible signal.
Noise Floor:	Below 70 dB with averaging.

Amplitude Linearity:	±1 dB or ±0.05% of full scale to 70 dB below full scale, whichever is greater.
Weighting:	Rectangular, Transient, Kaiser-Bessel or Hanning, selectable.
Processing:	1, 2, 4 or MAX transforms per memory period processing selectable in averaging modes.
Int/Diff:	Single and double integration and differentiation performed as post analysis operation on processed data. Results displayed and read out in correct engineering units.

1.6.3 Averager

Number of Averages (N):	1 through 2048 in any integer value. Averaged display always normalized.
Number of Averages (T):	Entered to the nearest second from 1 through 9999 secs. Averaged display always normalized.
Modes:	Linear, Exponential and Peak
Control (Local or Remote):	Start, Stop, Erase, +1, Auto Transient, and Transfer M1 to M2.
Domain:	Frequency — Averager memory M1 and M2 stores 400 lines of spectrum data or cross property information. Time — Averager memory stores 1024 time domain data values for each channel in LIN or EXPO modes. Utilizes sync reference input for triggering.

1.6.4 Transient Capture

Trans Arm (Local or Remote):	Sets transient capture circuitry to trigger on incoming data signal from CH A or CH B.
Threshold Level:	Keyboard entered as TH% of full scale input level for CH A or CH B.
Memory Hold (Local or Remote):	Independent control for CH A and CH B holds data signals in input memories.
Transient Averaging (Local or Remote):	Automatic sequence for averaging transient signals. Overloaded transients are automatically discarded from the process.
% Delay:	Delays, each channel, with respect to memory zero of that channel in 10% memory period steps.
Analysis:	Time waveform can be displayed and plotted from input memory, or the time waveform and corresponding spectrum can be performed with any of the four weighting functions.

1.6.5 System Functions: Computed and displayed for CH A and CH B

Real Time Spectrum
Averaged RMS Spectrum
Averaged Power Spectrum or Power Spectral Density
Sum, Difference, Ratio of RMS Spectrum or Power Spectrum
Equalized Ratio
Synchronous Spectrum
Synchronous Ratio

Cross Spectrum
Transfer Function
Equalized Transfer Function
Phase
Coherence

Coherent Output Power
Impulse Response

Time Mode
Normalized Autocorrelation
Normalized Cross Correlation

Probability Density Histogram
Probability Distribution

1.6.6 Display

Type: Built-in TV raster scan display.

Grids: Complete grid lines automatically generated for nonparallax viewing in LIN or LOG, X or Y format for single or dual display. Grid intensity — front panel adjustable.

Format: Single or dual channel, time or spectrum, cross-property magnitude and phase or coherence, real and imaginary, Co versus Quad, LIN or LOG vertical and horizontal selection.

List: Prompts raster display to show available data display combinations in selected function group.

Annotation: Identifies each data display as time RT, M1, or M2; control status including full scale input level, frequency range, average mode and number, X and Y parameters and cursor values.

Gain:

X Axis — LIN (X1) displays full 400 spectrum lines or full memory period of input time record. LIN X2 display 200 spectrum lines or 550% of input memory. LIN X4 displays 100 spectrum lines or 25% of input memory expanded over full display width. Data segment to be displayed selected by cursor position.

Y Axis — LIN gain of X0.1, X0.316, X1, X3.16, X10, X31.6, X100 for spectrum or time amplitude display. LOG gain up to +40 dB and attenuation of −20 dB in 10 dB steps. Gain factors automatically accounted for in data scaling.

1.6.7 CURSOR

Values:

X Axis — Reads seconds or milliseconds in time mode and Hz, KCPM, or Orders in frequency mode. Reads difference from a defined X axis reference.

Y Axis — Reads amplitude as V or EU in Time mode. Reads V dB, EU, PSD, or ΔP in Spectrum mode. Reads V or EU in the power spectrum mode. PSD (EU^2/Hz) readout and display automatically normalized to a 1 Hz effective noise bandwidth. dB values referenced to full scale or a set reference level defined through the keyboard. Phase read in degrees.

Modes:

Normal — Single cursor dot on either data trace.

Harmonic — Multiples of cursor fundamental are intensified with a true fine-tune alignment mode.

ΔX — Permits reading Δt or Δf values from a defined X-axis cursor reference.

ΔP — Provides digital calculation and display of RMS signal power from cell 1 to cursor location or between cursor frequency points defined in the ΔX mode.

ADRS — Enables cursor to be positioned to a specific cell location entered through the keyboard.

Mark — Provides capability of selecting and identifying, by number, up to 8 data points on single or dual display. Selected data points are intensified. Data values of X and Y parameters for all 8 data points can be listed on crt display.

Zero — Selectively replaces any data value in either input memory with a zero amplitude value under cursor control. Input memories must be in the HOLD mode.

Rotate — Selectively rotates, left or right, the contents of either input memory. Input memories must be in the HOLD mode.

1.6.8 Parameters

Panel:	Store and recall up to 7 operator defined front panel setups which are "remembered" when power is turned off.
PRGM:	Used for selecting Integration/Differentiation, Digital Plotter and Digital I/O Menus.
PLTR RATE:	Four different analog plotter rates can be selected through the keyboard.
AVG N:	Integer ensemble number up to 2048 entered through keyboard.
AVG T:	Average time, in seconds, up to 9999 entered through keyboard.
CHA, CHB:	Selected respective channel, or both, to which calibration values or setup parameters apply.
MV/EU:	Transducer sensitivity value for direct readout of engineering units.
LIN Ref:	Engineering unit reference number represented by a given voltage value.
TH%:	Transient capture threshold crossing as a % of full scale input level, for CH A or CH B.
% Delay:	Delays, both channels, with respect to the beginning of the memory, in 10% memory period steps up to 80 memory period intervals.
0 Offset:	Phase offset adjustable in 1 degree increments to a maximum of ± 180 degrees.
dB Ref:	dB reference level established through keyboard entry of data at selected cursor location on the Spectrum Display.
IDENT:	Provides up to a 4 digit display identification number.

1.6.9 Output

Video:	Composite video signal provides data and annotation for display on external raster scan monitor or video hard copy device; e.g., TEK 4632-6 or SD422.
Analog Scope:	Provides analog signal of X, Y and sweep trigger for displaying data trace only on external crt. (Optional)
X-Y Recorder:	Features Simulplot (continuous crt display during plot mode) and X-axis sweep rate control for automatic slowdown during plot of spectrum peaks. Analog X, Y and pen lift outputs. Plots contents of input memory or expanded part of input memory. Independent front panel position and gain control for the second data trace. Plots single or dual trace displays. Simple two-point CAL operation.

1.6.10 Built-In Option Specifications

1.6.10.1 Digital Translator (-1 Option)

Zoom Factors: 2, 5, 10, 30, 50, 100; front panel selectable

Zoom Accuracy: ±0.001% of full scale analysis range

Zoom Control: Established by cursor position. Cursor limits for each zoom factor are:

Zoom Factor	Cell Limits	
	Lower	Upper
2	50	350
5	20	380
10	10	390
20	5	395
50	2	398
100	1	399

Signal Gain: 1, 2, 4 or 8 times; front panel selectable

Digital Output: 200 digital words of floating point data transferred through -3B00 I/O option

Remote Control: All front panel XLTR controls plus cursor position can be remotely sensed and controlled through the -3B00 I/O option.

1.6.10.2 1/3 and 1/1 Octave Analysis (-2 Option)

Center Frequency and Band Numbers:

1/3 Octave

Center Freq. (Hz)	Band No.
1.6- 1,250	2-31
6.3- 5,000	8-37
12.5-10,000	11-40
25 -20,000	14-43
50 -40,000	17-46
100 -80,000	20-49

1/1 Octave

Center Freq. (Hz)	Band No.
2 - 1,000	3-30
8 - 4,000	9-36
16 - 8,000	12-39
31.5-16,000	15-42
63 -31,500	18-45
125 -63,000	21-48

Filter Characteristics:	Geometric mean frequency, effective bandwidth, and passband uniformity meet ANSI S1.11-1966 (R1975) Class III standards for 1/3 octave and Class II standards for 1/1 octave. These same parameters comply with IEC Publication 225.
Display Range:	1/3 Octave Mode — 30 full bands plus overall level 1/1 Octave Mode — 10 full bands plus overall level
Cursor Readout:	X-Axis — center frequency and band number Y-Axis — V, dB, dBR or Engineering Units (EU)
Analysis Time:	0.4 sec for 1/3 or 1/1 octave
Linearity:	±1 dB or ±0.1% of full scale, whichever is greater
Memories:	Two memories available for storing averaged spectra plus a third memory for displaying a real time spectrum.
Minimum Transmission Loss Variation:	±1 dB
Maximum Attenuation:	70 dB

1.6.10.3 Digital I/O (-3xxx Option)

I/O Interfaces

(1) IEEE 488 1978: Eight-bit parallel, byte serial with 3-wire handshake

- (a) Programmed talk/listen mode
- (b) Talk or listen-only — hardware or software selected
- (c) Device clear and service request implemented
- (d) Port control assignment — hardware or software selected

(2) EIA RS-232-C: Serial bit

- (a) Baud rate: 110, 300, 600, 1200, 2400, 4800, 9600, 19,200
- (b) Parity: Odd, even or none
- (c) Characters: 6, 7 or 8 bit with 1 of 2 stop bits
- (d) Format: ASCII or binary
- (e) Duplexing: Echo or quiet
- (f) Auto line feed: On or off
- (g) Handshake: Hardware or software
- (h) Port control assignment — hardware or software selected

Digital I/O Interface Compatibility Chart

I/O Designation	PDP-11 and Byte Format	IEEE 488	RS-232-C	HP - GL* Plotters	TEK 4662 Plotter*
-3D01	✓	✓	✓	✓	
-3D02	✓	✓	✓		✓

*Includes:
HP 7225A or B with 17601A (IEEE) or 17603A (RS-232-C) personality module;
HP 7220A (RS-232-C only — automatic four-color pen selection);
HP 7245A or B (IEEE only);
HP 9872B or C (IEEE only — automatic four-color pen selection).
**IEEE only

1.6.11 Miscellaneous

Operating Temp: 5°C to 45°C (40°F to 113°F)

Weight: 25 kg (55 lbs) Nominal

Dimensions: Width — 43,2 cm (17″)
Depth — 48,6 cm (19″)
Height — 26,7 cm (10.5″)

1.6.12 Power

105–125/210–250 Vac (switch selectable), 45–65 Hz at approximately 350 Watts.

SECTION II

THEORY OF OPERATION

2.1 GENERAL

Figure 2-1 shows the overall concept of operation of the Model SD375. The major functional sections of the instrument are controlled from the front panel, via the Z80 Microprocessor, through appropriate timing and control circuitry. Analog input data is conditioned, digitized and written into Input Memory. All subsequent processing is handled digitally. In the digital sections, tri-state bussing is employed throughout. Digital-to-Analog converters generate analog output signals for an external X-Y plotter. The following paragraphs provide a functional description of the SD375.

2.2 CONCEPT OF OPERATION

2.2.1 Timing and Control

The Timing and Input Control circuits generate the basic timing for the entire instrument: the clock for the Z80 Microprocessor control, the sampling frequencies for conversion, and appropriate timing for all internal data manipulation. All fundamental system timing is accomplished on the Timing and Control (A5A6) assembly.

2.2.2 Input Section

The time-domain analog input signal is applied to the Input Section where it is either attenuated or amplified to provide a normalized signal to the Low Pass Filter. The normalized input signal is passed through the low-pass filter so that components at higher frequencies cannot produce aliasing terms when analyzed in the frequency domain. The filtered analog signal is then amplified in the post-filter gain stage, sampled by a digital switch, and the derived samples are converted to 12-bit digital words. The word sequence is a digital representation of the applied analog signal. Most of the input section circuitry is contained on the Signal Conditioner (A5A1 and A2) assemblies and the 100 KHz Low Pass Filter (A5A3) assembly.

2.2.3 Input Memory

Alternate data samples from the Input Section are treated as "even" and "odd" samples. The "even" samples are used to produce the "real" component of a complexed word and the "odd" samples are used to produce the "imaginary" component of the complexed word. Consecutive "even" and "odd" samples are paired and stored in the 1024 $\times$ 14 bit Input Memory. The "even" samples are stored in the "real" section of the memory and the "odd" samples are stored in the "imaginary" section of the memory.

Figure 2-2 illustrates this operation. Paired real and imaginary samples are treated as complexed words (i.e., $S_0 + jS_1$; $S_2 + jS_3$; $S_4 + jS_5$; etc.) in the FFT algorithms employed by the CPU section.

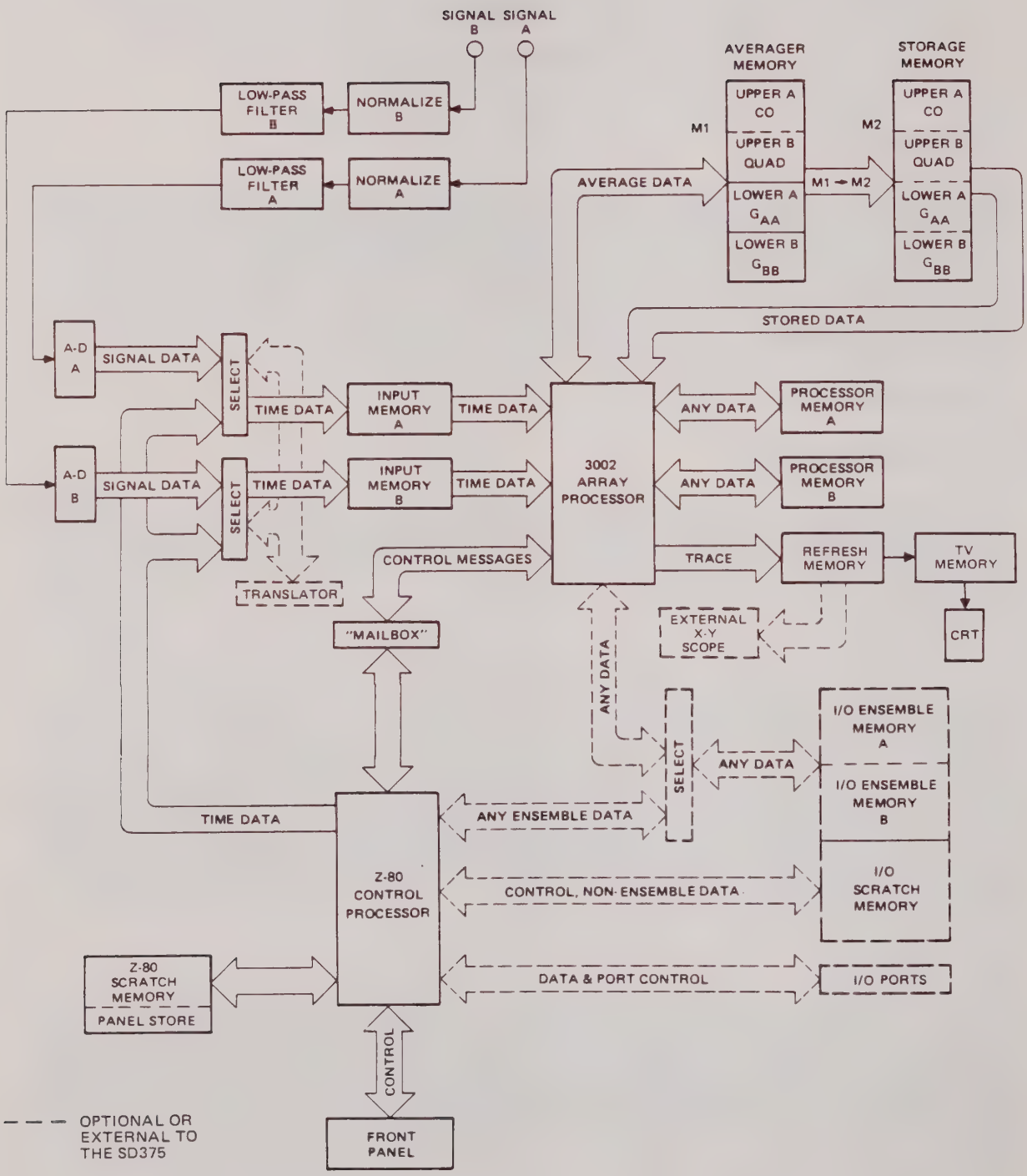

Figure 2-1. SD375 Conceptual Operation (Data Flow and Control)

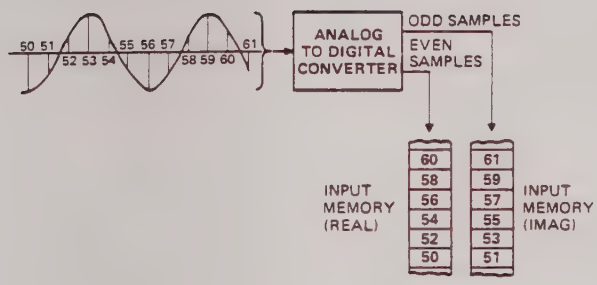

Figure 2-2. Typical Input Memory Organization

As directed by Microprogram Control, a block of 512 complexed contiguous words will be transferred from the Input Memory to the Processor Memory for processing by the CPU section. The block that is transferred consists of the most recent samples of the input analog signal.

2.2.4 Microprogram Control Section

This section provides the timing and sequence controls needed for controlling access to/from the Data Bus and for the processing functions performed by the CPU Section. It contains control PROM's which are capable of providing over 5000 24-bit machine language instructions. Front-panel Z80 Microprocessor control configurations, as well as the states of various circuits throughout the instrument, are monitored in order to control the sequence in which the instructions are fetched from the control PROM's.

2.2.5 CPU Section and Processor/Averager Memories

The CPU Section consists of a Central Processing Element (CPE) composed of eight bi-polar 2-bit slices; a hardware multiplier; RAM lookup tables for Sine and Cosine; and PROM lookup tables for Weighting, Square Root, EU-PSD, LOG X and LOG Y. This section performs all the required arithmetic and logical functions for the following operations:

a. A high-speed implementation of the Fast-Fourier Transform (with or without weighting).

b. Averaging of the real-time data stored in Processor Memory.

c. Computations for crt signal and Alphanumeric Display.

There are two Processor Memories which are functional elements of the CPU section. Each Processor Memory is a 1024 × 16-bit memory whose function is to store data during processing by the CPU Section. It also serves as a storage memory for the transformed, rectangular, and real-time data. The memories are used for each channel (when in a dual mode) or both are used for either channel (single channel mode). When used in the single channel mode, the memory becomes 2048 × 16.

There are two Averager Memories which are functional elements of the CPU section. Averager Memory 1 is a 1024 × 24 bit memory whose function is to store averaged or peak information depending on the Selected analysis mode (LIN or PEAK). Averager Memory 2 is also a 1024 × 24-bit memory whose function is to store the information from Averager Memory 1 for later use or for arithmetic functions between Averager Memory 1 and Averager Memory 2. An Extended Average Memory is used for performing floating point Sync Time Averaging. Processor and averager memories are contained on the (A5A13) assembly.

When a block of data is transferred from the Input Memory, the CPU multiplies the data by a weighting function (Hanning, Kaiser-Bessel, Transient and Rectangular) and stores the results in the Processor Memory. The CPU Section then computes the FFT. The resultant transformed data is then stored in the Processor Memory in rectangular format. Upon completion of processing, the contents of the Processor Memory is available to the Output Memory for display purposes.

If either the LIN, EXPO or PEAK mode has been selected, the CPU Section performs the selected operation on the real-time data from the Processor Memory and stores the results in Averager Memory 1. The contents of Averager Memory 1 are available to Averager Memory 2 and the Display Control Section for display. When data has been stored in this memory, it is retained until a new average or peak operation is initiated.

The contents of either the Processor Memory (real-time data) or the Averager Memory (Averaged or Peak data) may be selected for display by means of the front-panel PARAMETERS Group touch controls. When directed by the Microprogram Control Section, the CPU performs the required computations (depending upon the selected DISPLAY Y-GAIN) on the selected data to scale it for proper display. The data is then denormalized to 9 bits and written into a crt Refresh Memory in the Output Control and Display Section. When directed by the Microprogram Control Section, the CPU performs the required computations (depending upon the selected CURSOR Units) on the data at the cursor address. This data is then sent to the Video Interface assembly Character Generator to place an alphanumeric display of the frequency at which the cursor is located on the crt.

2.2.6 Output Control and Display Section

This section consists of all the circuitry, including timing and control, employed to display data on the crt and to provide for the remote, plotter and composite video outputs.

Output control PROM's provide the necessary instructions for accomplishing these functions. The status of the Z80 Microprocessor and several other circuits are monitored in order to control the sequence in which the instructions are fetched from the PROM's.

Digital X-axis data is generated by the output control and display circuitry and then converted to an analog signal. This analog signal is the normal (LIN X1) X-axis sweep signal. Expanded (X2 and X4) X-axis sweep signals are generated by using a DC $\propto$ Cursor Location signal to determine the portion of the normal sweep to be expanded. Either the normal or the expanded sweep signals may be selected for the X-axis by means of the front-panel Display X touch controls. The digital signal from an X-axis Counter also provides the read address information for the Refresh Memory.

The data in the Refresh Memory (frequency-domain) is loaded into TV Memory for display. Either this frequency-domain data or the digitized time-domain data from the Input Section may be selected for display on the TV by means of the front-panel PARAMETERS Group touch controls.

The cursor circuits employ up/down counters to generate either a NORMAL cursor or a HARMONIC cursor depending upon the position of the front-panel CURSOR Group touch controls. The counters are controlled by the CURSOR LEFT/RIGHT touch controls. The X-axis sweep is intensified when the count of the X-axis Counter is equal to the count of the Cursor Counter. This causes the cursor to appear on the crt as a square dot. When the dot is being moved across the crt display, a vertical line cursor is also generated and displayed along with the intensified dot. When HARMONIC cursor is selected, intensified dots are also placed on the X-axis sweep at all multiples of the fundamental cursor location. In this mode, the CURSOR LEFT/RIGHT touch controls can be used to position the fundamental cursor at any of 256 steps between adjacent cell locations. This provides finer resolution for aligning higher order harmonics. After the harmonics have been aligned, if the SET REF touch control is pressed, the intensified dots at the harmonic positions are frozen and a vertical line cursor is generated and displayed on the crt. This line cursor can then be moved to any of the 400 cell locations (512 cell locations for time) to allow a readout of the selected cursor data on the crt alphanumeric display.

When the PLOTTER mode is selected, a selectable clock pulse from the Timing and Input Control Section clocks the Cursor Counter continuously so that the cursor sweeps across the X-axis sweep on the crt. Each time the Cursor Counter and the X-axis Counter are equal, a Frequency Match signal is generated. This signal controls an X Sample-and-Hold and a Y Sample-and-Hold. The X-axis analog signal and the Y-axis analog data (frequency-domain) are applied to these Sample-and-Hold circuits. The outputs of these circuits are DC proportional to the data at the cursor location and are routed to the rear-panel PLOTTER X (J10) and PLOTTER Y (J11) connectors. A Sweep Rate Feedback circuit monitors the rate of change of the Y-axis data. When this rate exceeds a preselected slope, the sweep rate is reduced to allow sufficient time for the plotter to record the data peak.

2.3 TIMING AND CONTROL, DETAILED CIRCUIT DESCRIPTION

The development of basic timing for the SD375 is accomplished on the A5A6 PWA. Figure 2-3 depicts the functional operation of the timing circuitry. The detailed schematic drawing contained in Volume II (number 21046200) should be referenced whenever circuit specifics are desired.

2.3.1 Reference Oscillator

At the heart of the system timing is a 16.384 MHz crystal controlled reference oscillator (U40). Its output drives U75 to provide a 16 MHz clk complimented clock signal. The 16.384 MHz signal distribution is charted in the string list (see Appendix B).

All other required outputs are derived by division of the reference oscillator output.

2.3.2 Sampling Frequency Generator

The sampling frequencies for each of the different analysis ranges are developed within the timing chain by multiplexers U17 and U37 in conjunction with cascaded dividers U49, U46, U18, and U28. These circuits develop 21 different frequencies (each being 2.56 times the upper frequency limit of the selected analysis range) at the output of U37. Multiplexers U17 and U37 are feed ranging inputs from the front-panel touch controls via the Z80 microprocessor. The Z80 microprocessor senses changes in the selected frequency range and routes new data to the Z80 data bus to latches (A5A6, U26). The latch outputs (5 bits) are fed to multiplexers U17 (bits 1 and 2) and U37 (bits 3, 4, and 5).

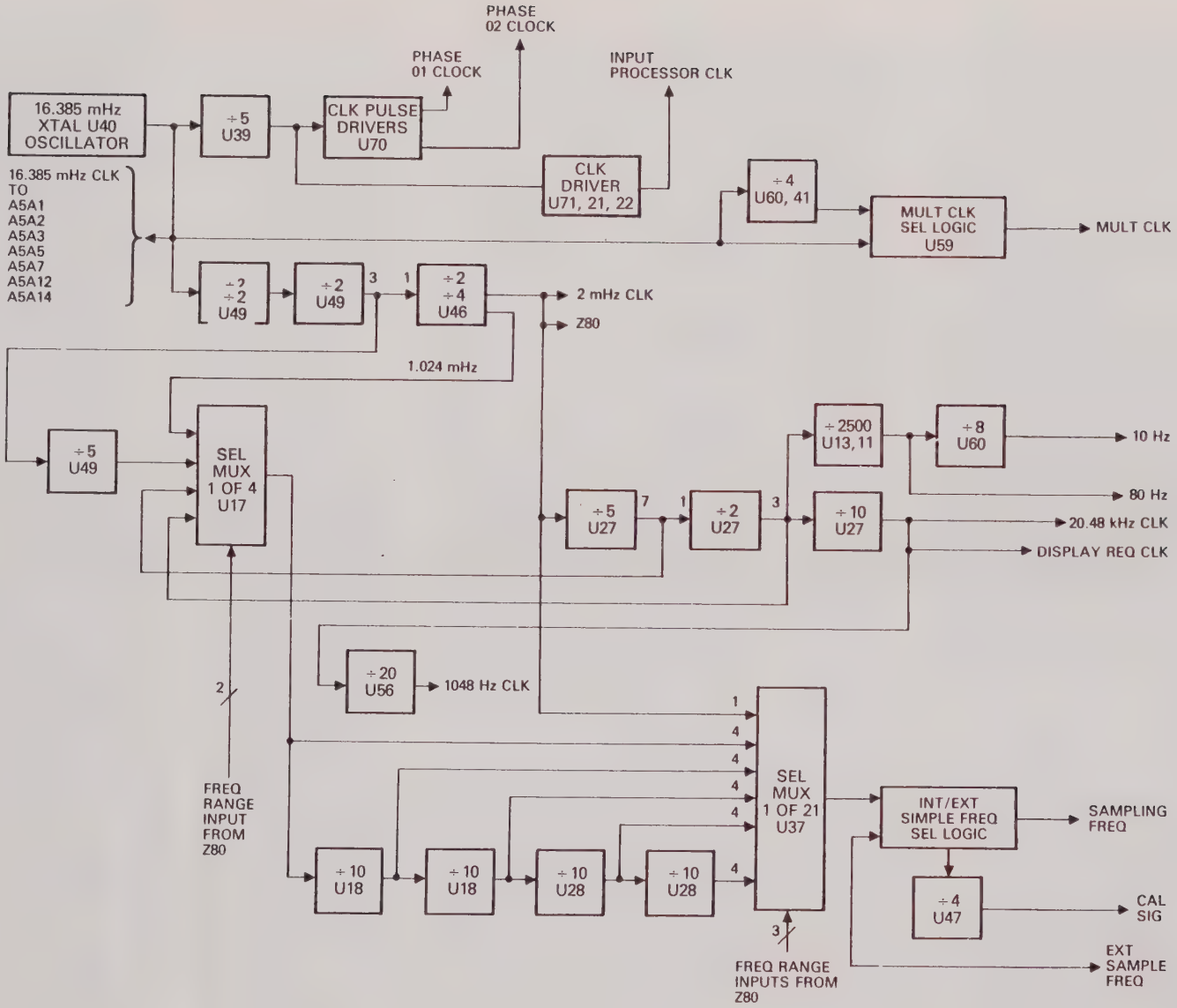

Figure 2-3. Timing and Control Assy (A5A6) Functional Block Diagram (System Timing)

The Internal/External Frequency Selector (U48) supplies the 21 internally generated sampling frequencies to the input signal conditioners or an external sample frequency source can be supplied by the operator via the Remote Sense/Control Connector (J22-9).

2.4 INPUT SECTION DETAILED CIRCUIT ANALYSIS

2.4.1 General

The Input Section of the SD375 consists of gain normalization circuitry (on the A5A1 and A5A2 PWAs), a low pass filter (A5A3), analog to digital conversion circuitry (on A5A3), and input memory (A5A7). The paragraphs which follow describe the input signal conditioning circuitry. The input memory is described in Section 2.5.

Because of identical circuitry incorporated in the Channel A and B Signal Conditioners, Channel A will be described in detail. The detailed circuit description is limited to major functional circuit elements comprising the input circuits as outlined in the Input Signal Conditioning Functional Block Diagram (Figure 2-12). Refer to detailed schematics when necessary.

2.4.1.1 Input Coupling

The signal to be analyzed is applied Signal Conditioner A (A5A1 PWA) from Input A (front panel) or J1 (rear panel) where it is dc or ac coupled to Common Mode Rejection circuitry. The coupling is always ac on input levels of 0.1 to 2V. On selected input levels of 5 to 20V either ac or dc coupling is selectable via the front panel ac touch control. The input coupling is controlled by relay K1 and driver Q1.

2.4.1.2 Common Mode Rejection

Amplifiers U11, 12, and 16 (Figure 2-4) are configured primarily to eliminate common mode error voltages which appear on the input BNC connector. This error voltage would be amplified along with the desired signal and result in error in the digitized signal output of the D/A converter. U12 amplifies the input signal plus the common mode error voltage and U11 amplifies the common mode error voltage. Their outputs are applied to U16 (operated differentially) where the effects of the common mode signal are cancelled and only the desired analog signal appears at U16's output. The input signal to the common mode rejection circuitry is divided by 2 when input levels of 0.1 to 2V are selected. When input levels of 5 to 20V are selected the input signal is divided by 20 prior to amplification.

2.4.1.3 Variable Gain Amplifier

The variable gain amplifier is basically a step attenuator yielding an output gain (A_o) proportional to the ratio of its feedback resistance (R_f) to its input resistance (R_i).

$$A_o = R_f/R_i$$

Selection of the input levels provides control voltages to the variable gain amplifier to select the appropriate input resistance (R_i) through an electronic switch.

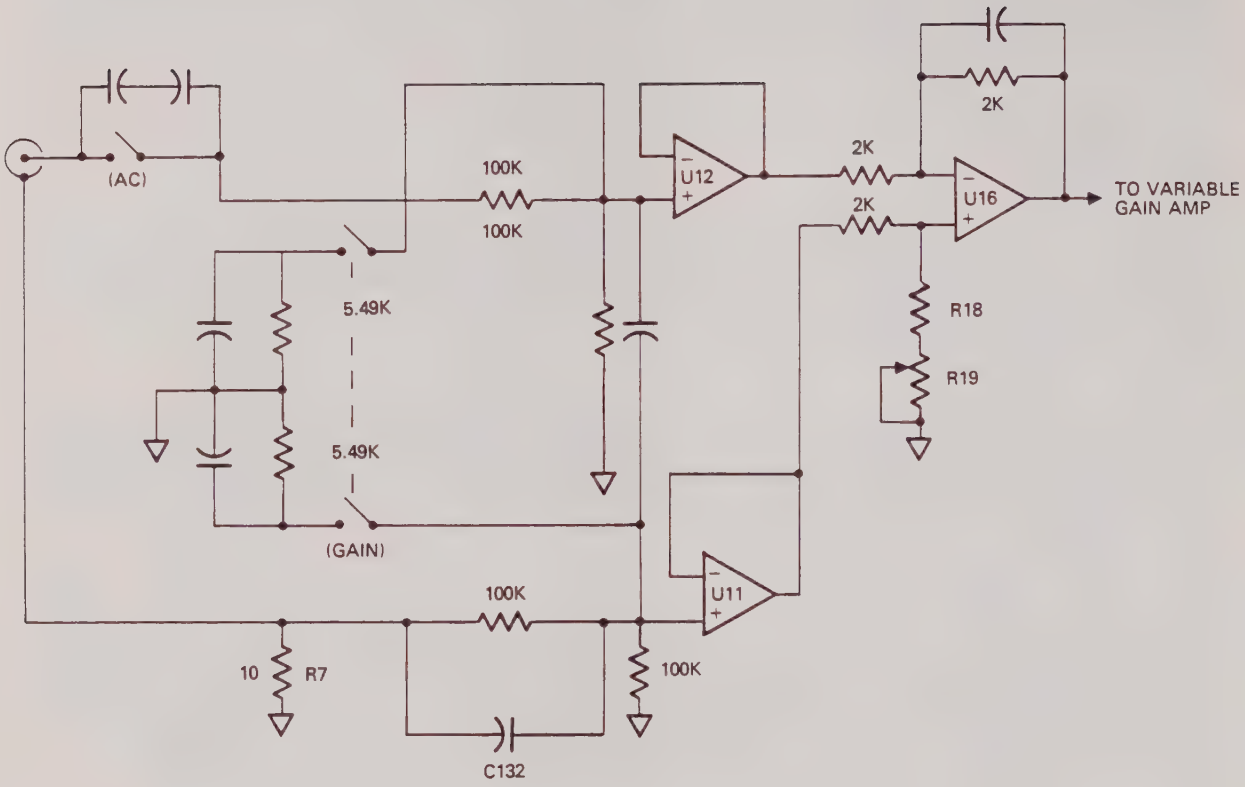

Figure 2-4. Simplified Differential Input Amplifier (Common Mode Rejection)

Figure 2-5 is a simplified schematic diagram of variable gain amplifier U8 with its associated control circuitry. Associated Variable Gain Amplifier circuitry include the input level PROM (A5A1 U53), level decoder (U51), drivers (U37, U38), the Level Attenuator Select Switch (U52) and an R/C network.

Level inputs from the Timing and Control PWA (A5A6) are fed to Level PROM (U53). Its outputs are read by level decoder (U51) and decoded to connect one of 8 possible input resistance networks to the summing point (U8-2) through drivers U37 and U38.

Input level voltages are also fed from U53 to the electronic switch where they are converted and decoded to provide a gated bias voltage to each switch.

The analog switch is shown in Figure 2-6, with grounding contact made through an open collector inverter. The summing junction is made through a P-channel FET. The P-channel FET characteristics are such that it can be driven from near TTL logic levels. The inverter and FET have a common drive signal, however, the FET requires a more positive level than the inverter, so a pull-up resistor is added. Since the FET is connected to a summing junction, its source and drain are close to zero volts, therefore, a +3.5V level is required to hold it off. Also, since the FET "on resistance" is in series with the operational amplifier input impedance, the FET resistance does not affect the selected gain.

Grounding of the unused resistor networks by the open collector inverters prevents signal feedthrough across the stray capacitance of off FETs. This preserves a flat frequency response at all attenuator settings.

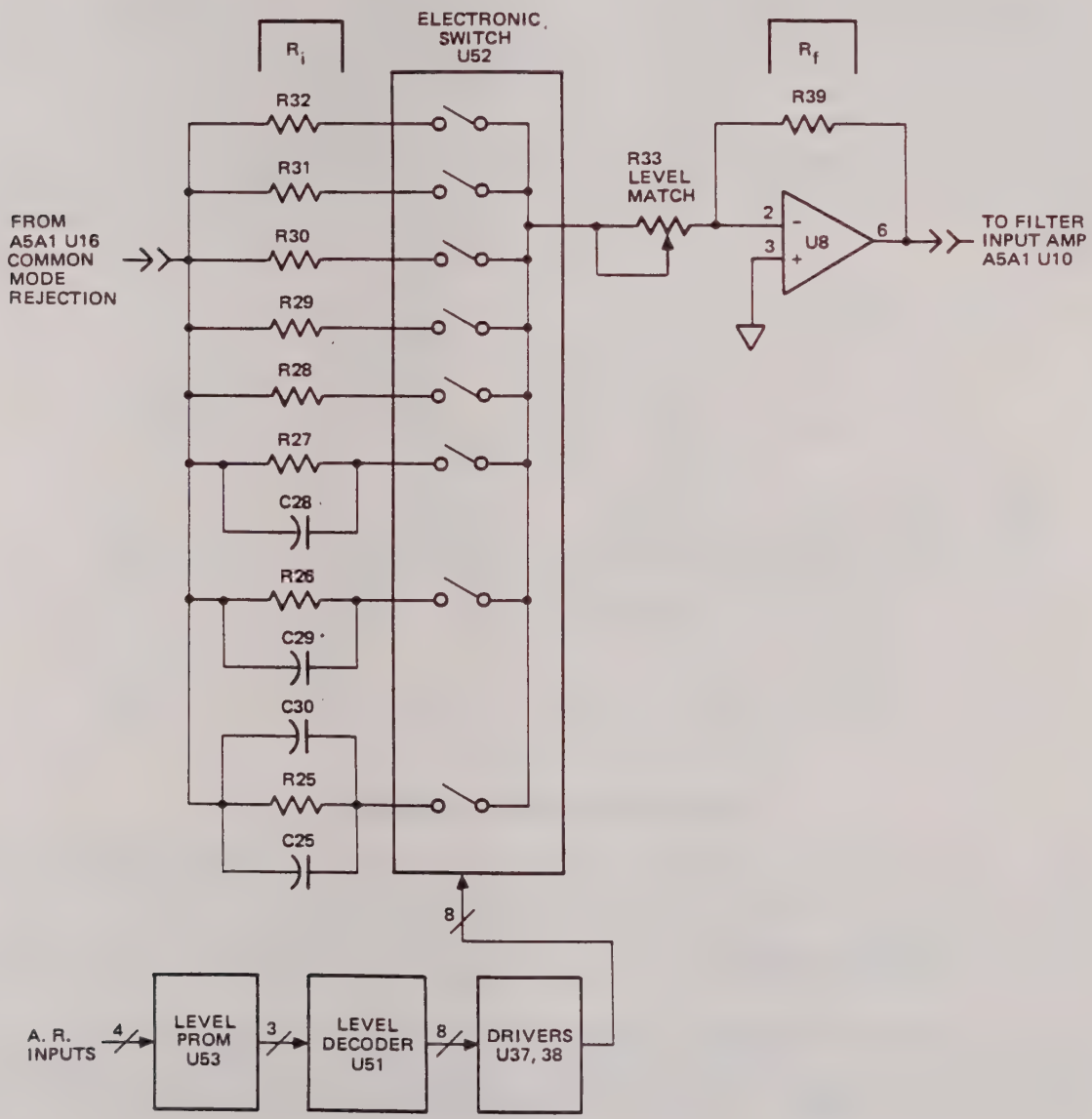

Figure 2-5. Simplified Variable Gain Amplifier

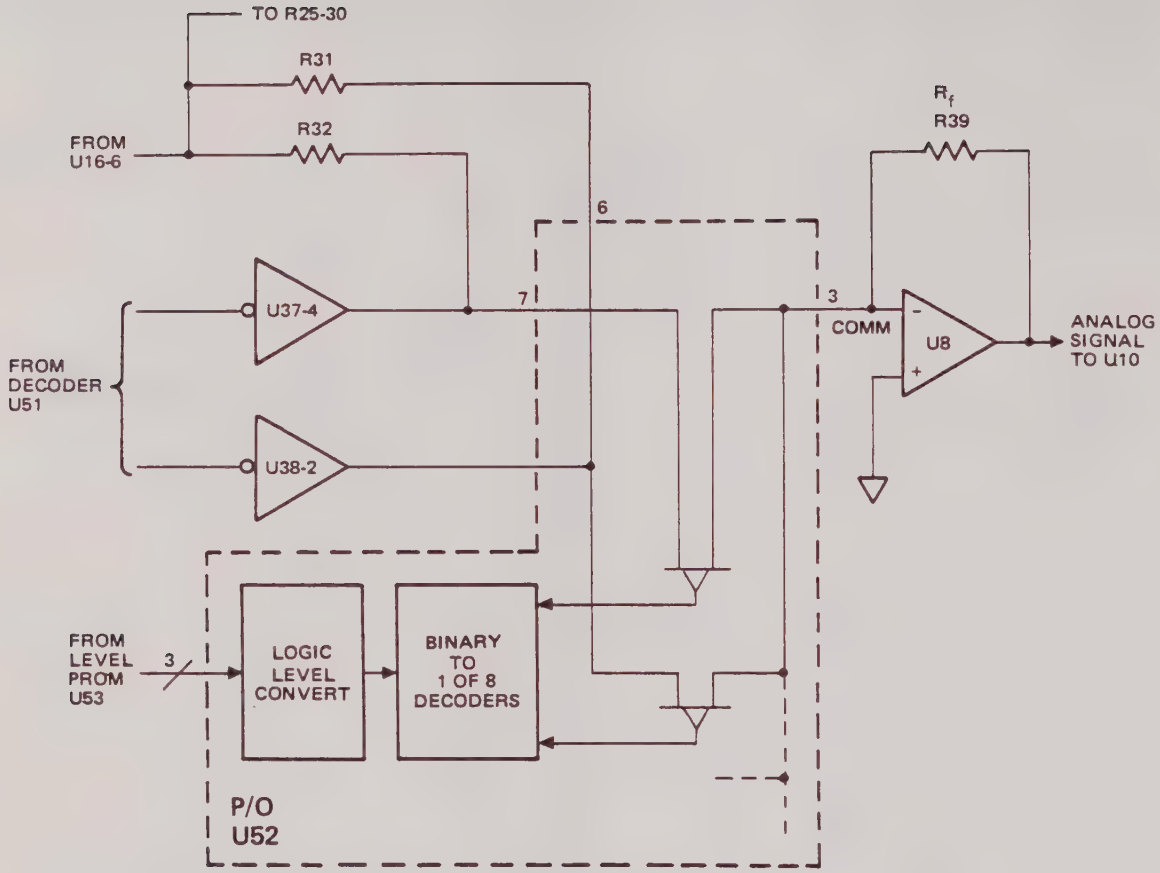

Figure 2-6. Simplified Analog Switch

Amplifier U10 is the Filter Input Amplifier and provides a fixed amount of Gain to the input signal before it is applied to the low pass filter via the Cal/Sig Select relay (K2).

2.4.1.4 Cal/Signal Select Circuitry

Relay Driver Q4 and relay K2 will select the input signal or the Cal signal (stored at cell 260 in processor memory) to be processed. Depressing the TEST touch control of the front panel Input Group supplies the selected Cal signal to the Signal Conditioner and it is processed as if it were an externally applied analog input.

The normalized signal at the output of U10 is fed through K2 to the Low Pass Filter I-IV.

2.4.2 Low Pass Filter (I-IV)

2.4.2.1 Frequency Filtering

The Low Pass Filter circuitry is employed to filter out (attenuate) those frequency components in the input signal that are greater than 1.56 times the selected analysis range. Frequency components higher than the selected range must be filtered out before being analyzed to prevent them from appearing as lower frequencies (aliasing terms). See Figure 2-7 as an example. When set to the 200 Hz range, if a 350 Hz signal is allowed to be analyzed, it will appear to be a 175 Hz signal. As shown in the figure, the higher frequency contained in the input signal actually completes 2 cycles while the analysis sample points falsely identify the signal as one cycle (i.e., a lower frequency). These false frequencies are called aliasing terms. To minimize their occurrence, the Low Pass Filter establishes a filter cutoff frequency using the selected frequency range set on the RANGE, FREQ touch controls.

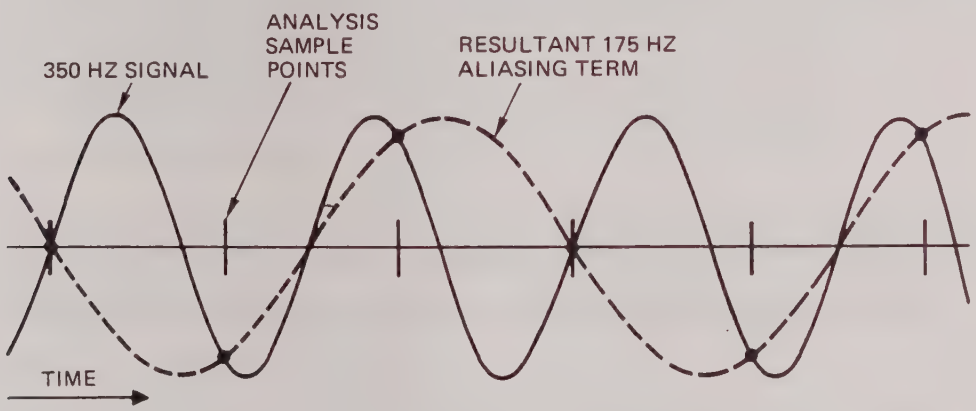

Figure 2-7. 175 Hz Aliasing Term

2.4.2.2 Elliptic Filters

The Elliptic Filter is a low pass filter designed using elliptic polynomials. It has seven poles and six zeroes. The cutoff frequency of the filter (f_c) is equal to 1.0 times the selected analysis range (see Figure 2-8).

The seven poles and six zeroes are generated by cascading four sections. One section generates a real pole and the other three sections each generate a pair of complex poles and complex zeroes. Each of the latter three sections is made up of three operational amplifiers connected in a modified bi-quad configuration (see Figure 2-9).

In the circuit of Figure 2-9, the components are selected so that $R_6 = R_4 = R_5$; $R_1 = R_2 = R$; $R_3 = QR$; and $C_1 = C_2 = C$. The filter cutoff frequency is controlled by varying R in increments of 1, 2, 4, and 8 or by varying C in multiples of 10. Thus, anything that does not vary with decade changes is resistor related, whereas anything peculiar to a decade multiplier is capacitor related.

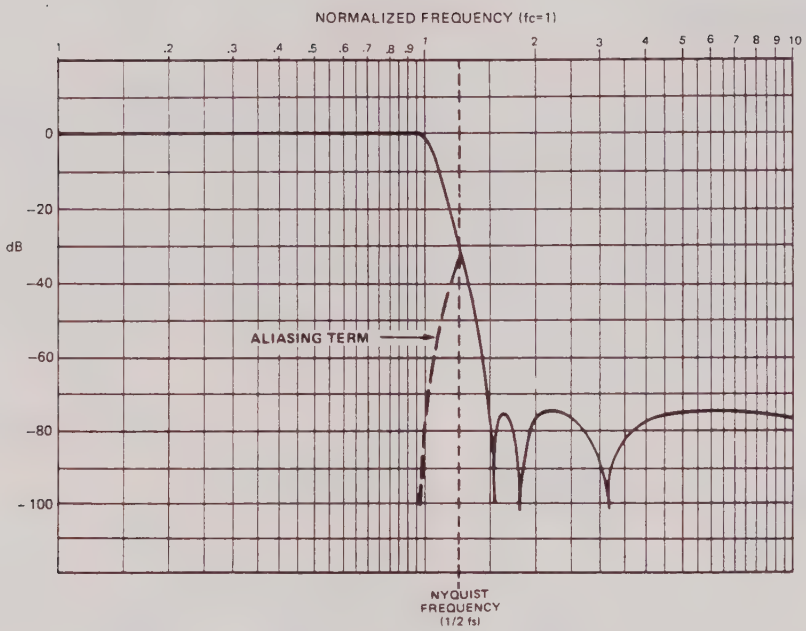

Figure 2-8. Typical Elliptical Filter Amplitude Response (Showing Aliasing Term)

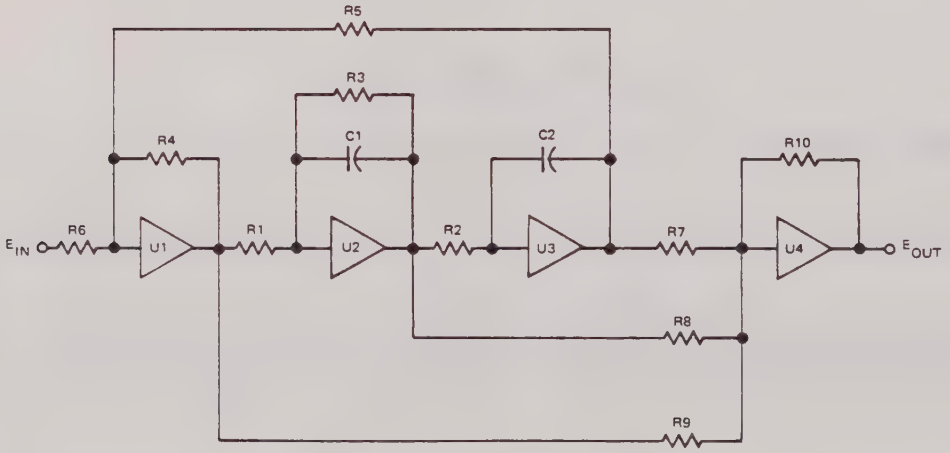

Figure 2-9. Simplified Bi-Quad Elliptical Filter Configuration

2.4.2.3 Low Pass Filter

The Low Pass Filter is designed using elliptic polynomials. It has seven poles and six zeros. Its cutoff frequency is determined by analysis ranging inputs from the front-panel RANGE, FREQ touch controls which control 14 different electronic switches to select various circuit configurations which produce the required low pass characteristics. Its typical performance is 0.2 dB P-P ripple in the pass band and 70 dB minimum rejection in the stop band reached at 1.56 f_c. The seven poles and six zeros are generated by cascading four sections. Each section generates a pair of complex poles and each of the first three sections generates a pair of complex zeros. Each section is made up of three operational amplifiers connected in a modified bi-quad configuration.

2.4.2.4 Low Level Signal Enhancement

At the input to the first stage of the Low Pass Filter, the Sine Dither square wave is summed into the signal. This square wave produces a single tonal that is outside the band and therefore does not appear in the output. Its purpose is to enhance the resolution of low-level signals to the A/D Converter.

2.4.3 100 KHz Low Pass Filter

2.4.3.1 Low Pass Filter Signal Select

On the 100 KHz Analysis range the I-IV Low Pass filter is bypassed by the 100 KHz Low Pass Filter via the signal select relay A5A1 K11. This relay is energized by driver A5A1 Q16 when the SD375 operator selects the 100 KHz range.

2.4.3.2 100 KHz Low Pass Filter

The 100 KHz Low Pass Filter operates very similar to the Bi-Quad Elliptical Filter described in Section 2.4.2.

2.4.4 Post Filter Gain Amplifiers

The selected low pass filter output signal is coupled through A5A1 C95-C96 (ac) to A5A1 Q13 to post filter gain amplifiers (A5A1 U13, U17) where, in addition to amplification, a random dither is summed with the signal. The Random Dither circuit (Q8, VR7 and associated components) generates a statistically controlled noise signal (white noise) which is summed with the filtered signal to eliminate the effects of harmonics introduced by the Sine Dither signal (back in the Low Pass filters) and to enhance the analog to digital converter resolution of low level input signals.

2.4.5 Analog-to-Digital Conversion

2.4.5.1 General Description

The Sample and Hold circuit samples the selected signal at the sampling clock (f_s) rate and the samples are applied to the A/D Converter. This is an ultra-high-speed 12-bit successive approximation converter which is completely self-contained including a high-speed comparator, a high-speed D/A, successive approximation register, 6 MHz clock, reference source, and steering logic. At the end of conversion of each

input sample, the A/D Converter provides a Conversion Complete signal to the Timing and Control Circuits, the Input Overload circuits, the Transient Capture Trigger Pulse Generator, the optional Translator circuits, and the Input Memory circuits. If the level of the input sample is such that the converter starts clipping, it produces an overload output which is routed to the Overload Logic. The 12-bit output of the A/D Converter is a digital representation of the input analog signal and is loaded into the A/D latches by the Conversion Complete signal from the A/D Converter. The digital data in the A/D latches is sampled filter data and the Input Control Section writes it into the Input Memory. If the optional Translator is used, the data in A/D latches is sent first to the optional Translator circuitry. After the translation process is completed, the data is sent to the Input Memory. When the data is read out of Input Memory, it is loaded into the Memory Output Latches. The Memory Output Latches have tri-state outputs which are controlled by the Microprogram Control Section.

2.4.5.2 A/D Timing and Control

When analysis ranging information is placed on the Z80 data bus, the Timing and Control PWA (A5A6) generates one of 21 discrete sampling frequency (f_s) outputs which is fed to Signal Conditioner A (A5A1). The Sampling Frequency (which is 2.56 times the upper frequency limit of the selected analysis range) is used to clock flip-flop U66 whose output controls U67 Sample and Hold IC.

2.4.5.3 Sample and Hold

U67 and U70 comprise the S/H, SAR Voltage Ref, Current Ladders and Generators and Comparator which comprise the A/D circuitry.

2.4.5.4 Successive Approximation Register

The U70 VLSI chip consists of the Resistor Networks, SAR Registers, Voltage Ref, Comparator and Internal clocking circuitry.

2.4.5.5 Digital Encoding Circuit

The successive approximation Digital Encoding circuit employs redundant bit correction. The digitizing circuitry encodes a binary number whose value is proportional to the sampled signal from the Signal Conditioning circuitry, and indicates whether the sampled signal exceeds the range of the digital encoder. The sampled signal is summed with a 10 volt reference within the comparator (U70). This converts the bipolar signal into a positive uni-polar signal. The successive approximation logic varies the Current Generator (U70), and the Comparator then determines if the resulting voltage is larger or smaller than the offset input voltage. The current is varied in sequential increments and the Comparator determines which of the increments are smaller than the input. The successive approximation logic latches these increments and the logic outputs are then added and transferred to the storage registers. The output word is compared to an overload level by the A/D Overload Logic (A5A1 U50, U48) and A5A1 U33.

2.4.5.6 D/A Feedback

The Internal analog representation of the digital approximation is developed within U70 (a 12-bit high speed A/D converter). Offset errors of U70 may be minimized with the adjustment of Variable Resistor R9.

Figure 2-10 shows the Internal operation of U70. The MSB is initially set to zero and other all bits are initally turned on.

The bits are determined in succession, starting with the MSB Bit 1. Then each bit will be valid for 26 ns after each clock pulse.

The clock pulses are internally generated within U70. The clock is turned on when Convert Command is High. When Convert Command is Low, clock is inhibited.

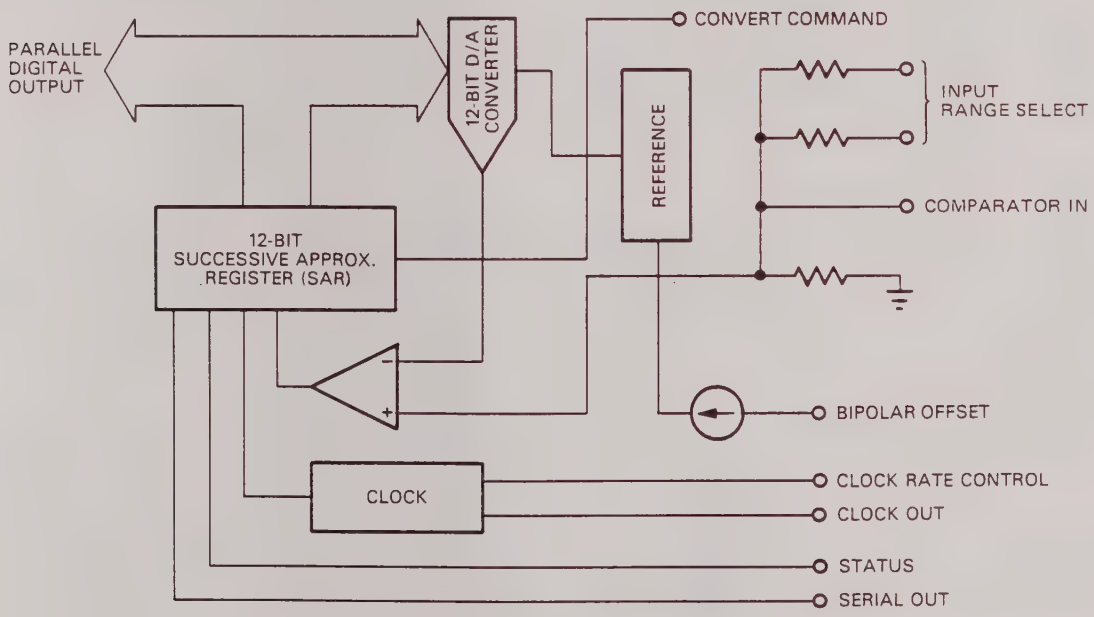

Figure 2-10. Differential D/A Feedback

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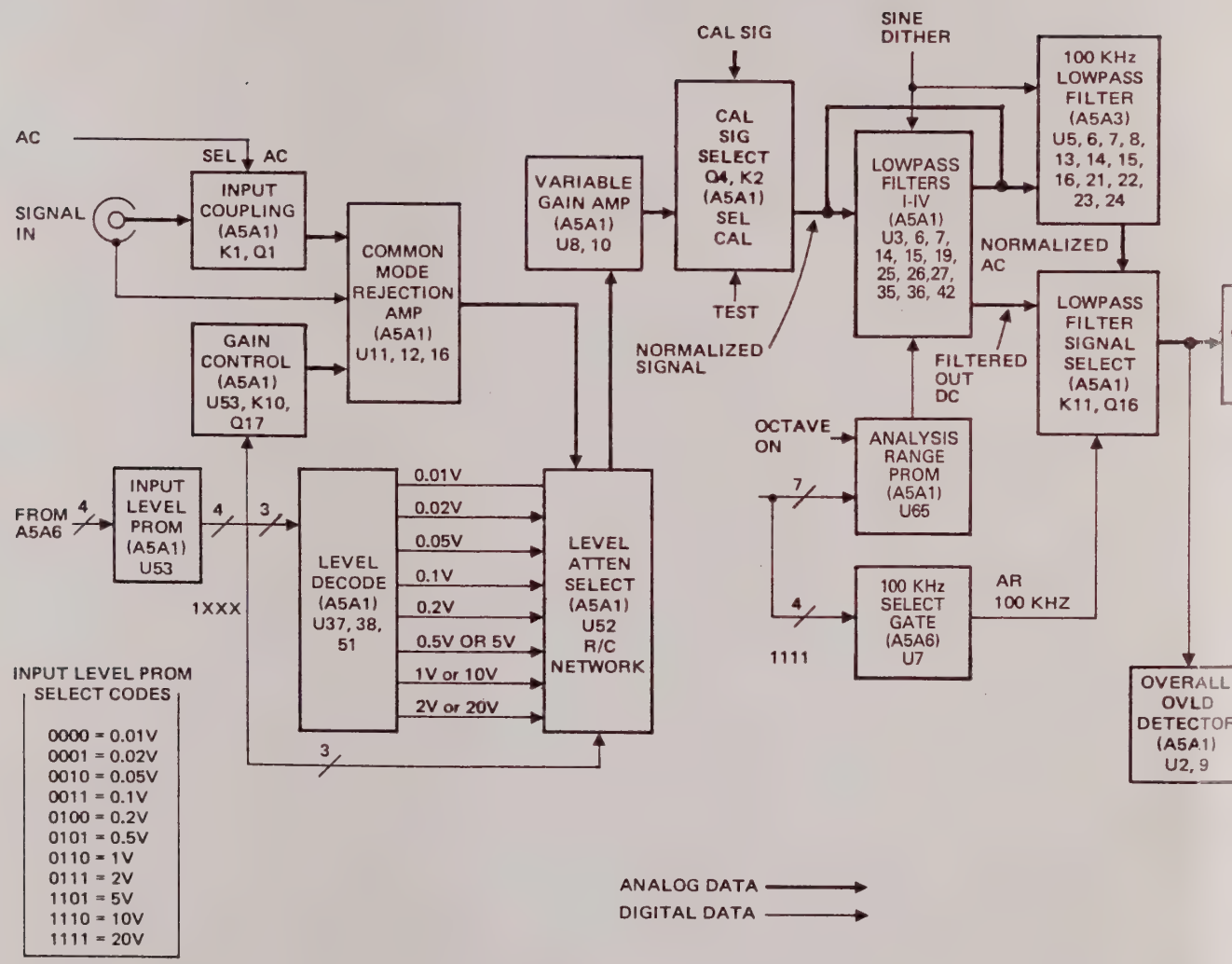

AC
SEL
AC
SIGNAL IN
INPUT COUPLING (A5A1) K1, Q1
COMMON MODE REJECTION AMP (A5A1) U11, 12, 16
GAIN CONTROL (A5A1) U53, K10, Q17
VARIABLE GAIN AMP (A5A1) U8, 10
CAL SIG
CAL SIG SELECT Q4, K2 (A5A1) SEL CAL
TEST
NORMALIZED SIGNAL
SINE DITHER
LOWPASS FILTERS I-IV (A5A1) U3, 6, 7, 14, 15, 19, 25, 26,27, 35, 36, 42
100 KHz LOWPASS FILTER (A5A3) U5, 6, 7, 8, 13, 14, 15, 16, 21, 22, 23, 24
NORMALIZED AC
LOWPASS FILTER SIGNAL SELECT (A5A1) K11, Q16
FILTERED OUT DC
OCTAVE ON
ANALYSIS RANGE PROM (A5A1) U65
FROM A5A6
4
INPUT LEVEL PROM (A5A1) U53
4
3
1XXX
LEVEL DECODE (A5A1) U37, 38, 51
0.01V
0.02V
0.05V
0.1V
0.2V
0.5V OR 5V
1V or 10V
2V or 20V
LEVEL ATTEN SELECT (A5A1) U52 R/C NETWORK
3
7
4
1111
100 KHz SELECT GATE (A5A6) U7
AR 100 KHZ
OVERALL OVLD DETECTOR (A5A1) U2, 9
INPUT LEVEL PROM SELECT CODES
0000 = 0.01V
0001 = 0.02V
0010 = 0.05V
0011 = 0.1V
0100 = 0.2V
0101 = 0.5V
0110 = 1V
0111 = 2V
1101 = 5V
1110 = 10V
1111 = 20V
ANALOG DATA
DIGITAL DATA

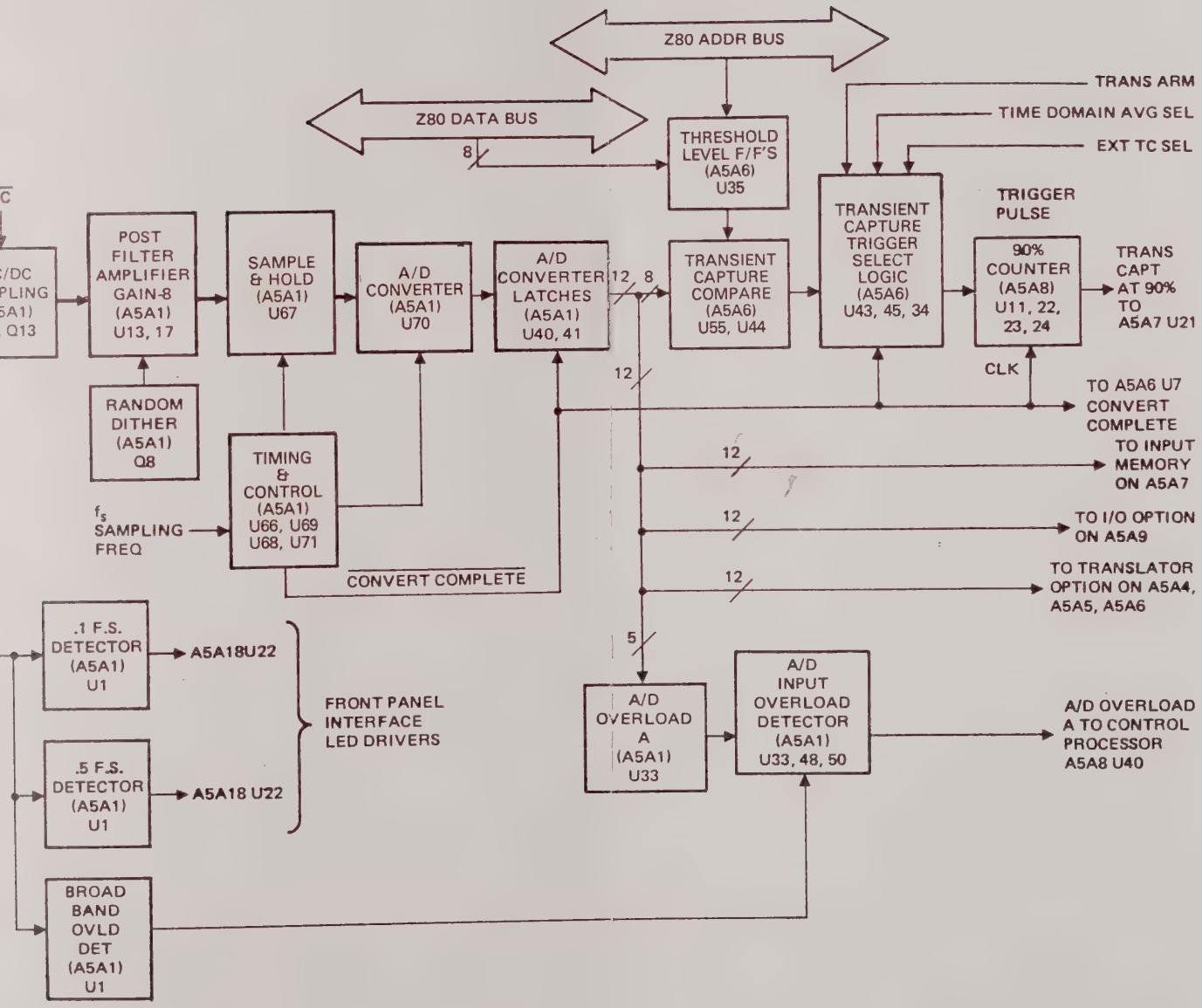

Z80 ADDR BUS
Z80 DATA BUS
8
THRESHOLD LEVEL F/F'S (A5A6) U35
TRANS ARM
TIME DOMAIN AVG SEL
EXT TC SEL
TRANSIENT CAPTURE TRIGGER SELECT LOGIC (A5A6) U43, 45, 34
TRIGGER PULSE
90% COUNTER (A5A8) U11, 22, 23, 24
TRANS CAPT AT 90% TO A5A7 U21
CLK
POST FILTER AMPLIFIER GAIN-8 (A5A1) U13, 17
SAMPLE & HOLD (A5A1) U67
A/D CONVERTER (A5A1) U70
A/D CONVERTER LATCHES (A5A1) U40, 41
12, 8
TRANSIENT CAPTURE COMPARE (A5A6) U55, U44
RANDOM DITHER (A5A1) Q8
TIMING & CONTROL (A5A1) U66, U69 U68, U71
f_s SAMPLING FREQ
CONVERT COMPLETE
12
TO A5A6 U7 CONVERT COMPLETE
TO INPUT MEMORY ON A5A7
TO I/O OPTION ON A5A9
TO TRANSLATOR OPTION ON A5A4, A5A5, A5A6
5
.1 F.S. DETECTOR (A5A1) U1
A5A18U22
.5 F.S. DETECTOR (A5A1) U1
A5A18 U22
FRONT PANEL INTERFACE LED DRIVERS
BROAD BAND OVLD DET (A5A1) U1
A/D OVERLOAD A (A5A1) U33
A/D INPUT OVERLOAD DETECTOR (A5A1) U33, 48, 50
A/D OVERLOAD A TO CONTROL PROCESSOR A5A8 U40

Figure 2-11. Input Signal Conditioner Functional Block Diagram

2.5 INPUT MEMORY SECTION DETAILED CIRCUIT DESCRIPTION

2.5.1 General Concept

The primary purpose of Input Memory is to provide storage for the digital data sampled by the input signal conditioning circuits. The Input Memory circuits are located on the A5A7 PWA. These circuits control the read and write operations of the Input Memory. These circuits are controlled by signals from the Input Section and from the Microprogram Control Section. Figure 2-14 is a functional block diagram of the Input Memory and its control circuits.

To understand the operation of the Input Memory Control circuits, it is first necessary to understand the timing relationships between the three primary controlling signals. These signals are (1) *Input Request*, (2) *Conversion Complete* and (3) *Program Complete*. The Input Request signal is generated by the Microprogram Control Section each time the processor memory is ready to receive a new ensemble from Input Memory for processing, which represents 1024 contiguous 12-bit data words to be stored in the input memory.

As directed by Microprogram Control, a block of 1024 words (conceptually considered as 512 Real and 512 Imaginary words) are transferred to Processor Memory for further processing by the CPU Section.

This operational sequence continues until the number of ensembles sampled (selected by the front-panel AVG N touch controls) has been processed.

When the CPU has completed reading the Input Memory (one complete ensemble) to generate the spectrum, the Microprogram Control Section will generate a Program Complete signal. Conversion Complete is generated by the A/D Converter, at one-half sampling rate (f_s), each time a sample has been converted to a digital word and is ready to be written into Input Memory. Since the sampling rate is dependent upon the selected frequency range, the Conversion Complete signal can occur at any time and at various frequencies in relation to the Input Request Signal. One or more Conversion Complete signals could occur during the burst of 1024 Input Requests from the CPU. Each time a Conversion Complete signal does occur, unless the Input Memory is in HOLD, the converted sample must be written into Input Memory before the next Conversion Complete signal occurs.

2.5.2 Logic Controller

The Input Memory is a microprocessor based data storage device which operates under primary control of the control processor (A5A8). The heart of the Input Memory PWA is its logic controller which consists of five (5) PROMs. The PROMs are programmed to provide microinstructions for all required Input Memory tasks and/or subroutines. Instructions are permanently stored by four of the PROMs and are addressed by the Stored Address Information in INPUT PROM 11 (A5A7U3) NEXT ADDRESS SELECT. (See Figure 2-13.)

Next Address Select U3 (like all other PROMs used on the A5A7 PWA) is a 256 word by 8-bit programmable Read Only Memory. It is arranged so that its output is latched onto the address bus by U88 and simultaneously felt by INP11, INP12, INP13, INP14 and INP 15 PROMs. The latched ADDRESS BUS drives U3 to the NEXT ADDRESS which will appear on the address bus only when the input processor clock occurs. All five PROMs are programmed with the same address map.

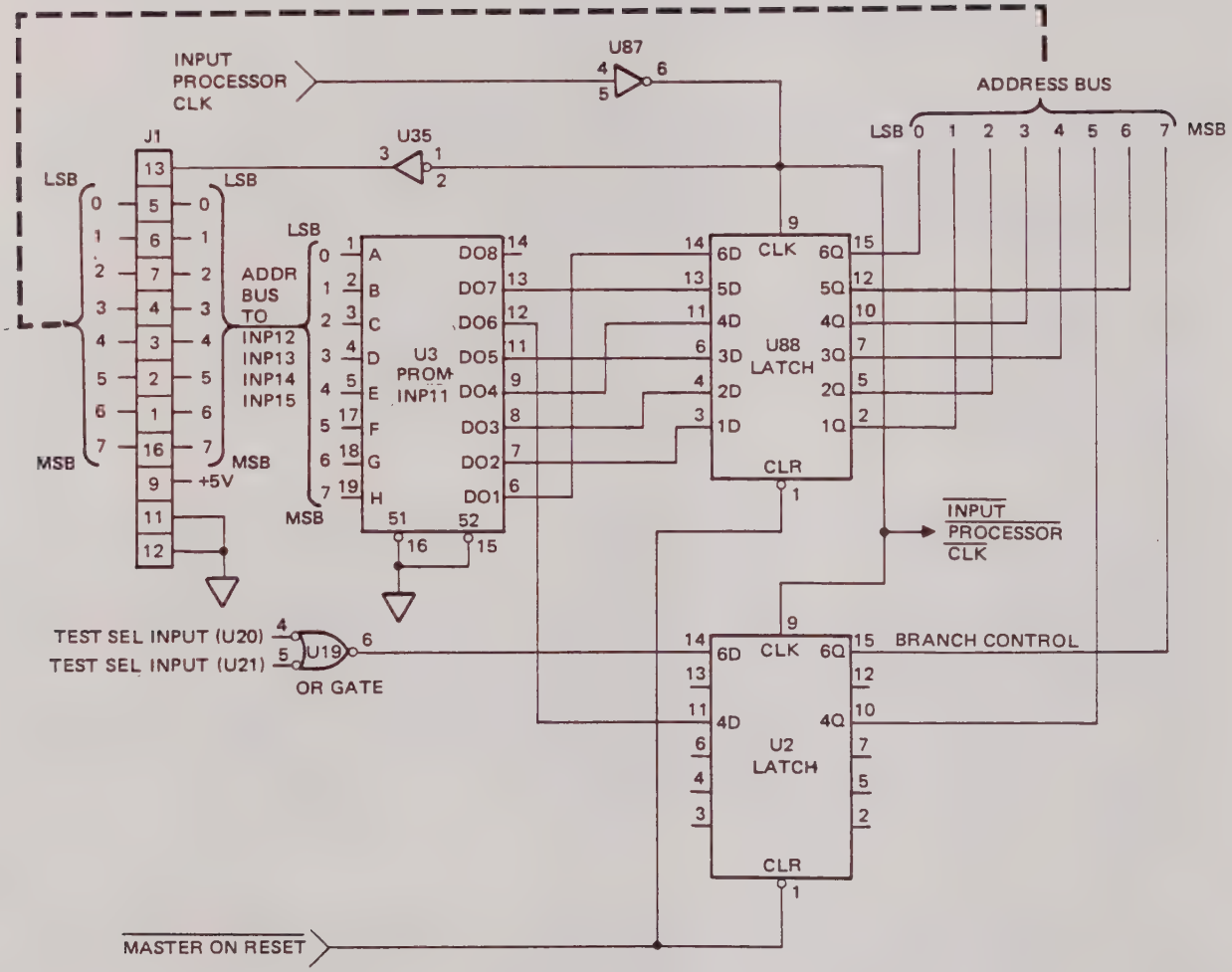


Figure 2-12. Input Memory Assembly Logic Controller Address Generator

The Master-On Reset signal from the 100 kHz Low Pass Filter and Plotter PWA (A5A3) to U88, U2 and U52 initializes the array processor (INP11 PROM) U3 at address 00. This is the point at which the program is entered. From this point, the sequence in which the instruction words are fetched from the PROM is determined by testing various inputs to the Test Selector (U20, U21). The inputs to be tested are determined by data select inputs to the Test Selector from INP12 PROM (bits 4 through 7).

Primary timing is accomplished with an input processor clock from the Control Processor (A5A8) card. Input processor clock pulse are fed to latches U2, U7, U88, U89 and the Test Selector (U20, U21).

INP11 (the NEXT ADDRESS selector) is incremented sequentially unless otherwise directed by its output plus the state of U2-6Q. U2-6Q is set with the positive transition of the input processor clock pulse if the U2-6D and CLR inputs are held high. U2-6D goes on the Address Bus as MSB and is fed back to the input of INP11. The MSB is used to range to addresses above 128.

The next address appearing on the ADDRESS BUS will be whatever is stored (programmed) at the location addressed. The 8-bit address is decoded by INPUT 12, 13, 14 and 15 to set up logic levels required (mode controls, gating instructions, etc.) for the various circuits of the Input Memory (A5A7) PWA.

2.5.3 Source Selection Logic

The Source Selection Logic circuits accept inputs from the Z80 via the Z80 data bus and data input buffer U52 (see Figure 2-13) before being applied to Source Decoders U50, U51 and Source Selectors U47 and U48.

The primary purpose of source selection logic is to (1) determine which of six possible data sources will be processed to input memory, (2) enable appropriate input data buffers, and (3) cause the callup of appropriate instructions that will write the input data into memory.

2.5.3.1 There are six sources of inputs to Input Memory and they are as follows:

a. Channel A A/D

b. Channel B A/D

c. Translator A

d. Translator B

e. Z80 data

f. Nobody writes (memory in hold)

2.5.3.2 Input Data is decoded by gates U49, 53, 36, 54, the translator data input registers, Channel A or Channel B A/D converter input memory buffers or the Z80 data input buffers.

2.5.3.3 The writing of data into input memory is accomplished by setting either WRITE REQ A or B flip-flops with a signal from the data input source. These signals are tested by Source Selectors U47 and U48 and are known as:

a. +5 volt (nobody writes)

b. Z80 Data Input

c. XLATOR RDY

d. A CONVERT COMPLETE

e. B CONVERT COMPLETE

The states of the WRITE REQ A and/or B flip-flops are fed to the Logic Controllers Test Selector.

2.5.4 Read/Write Counters

The Read and Write Counters are identical 10-bit synchronous binary counters which count up to 1024 (the cycle length required to process one complete ensemble).

There are Read and Write Counters for each of the two Memory Sections (A and B) which operate for Channels A and B repectively. The Read and Write Counters feed a selector with is enabled for read or write by SEL READ CTRS (a latched gate fed from INP13 PROM through latch U89).

Both Read Counters (A and B) receive a load gate (EXECUTE), and are incremented by (INC READ CNTRS) from Command Decode Selector (U8, U9).

The Write Counters A and B are enabled by LD WRITE CNTR A or LD WRITE CNTR B respectively from the Command Decode Selector U8, U9. The Write Counters are incremented by Command Decode Selector (U8, U9) outputs.

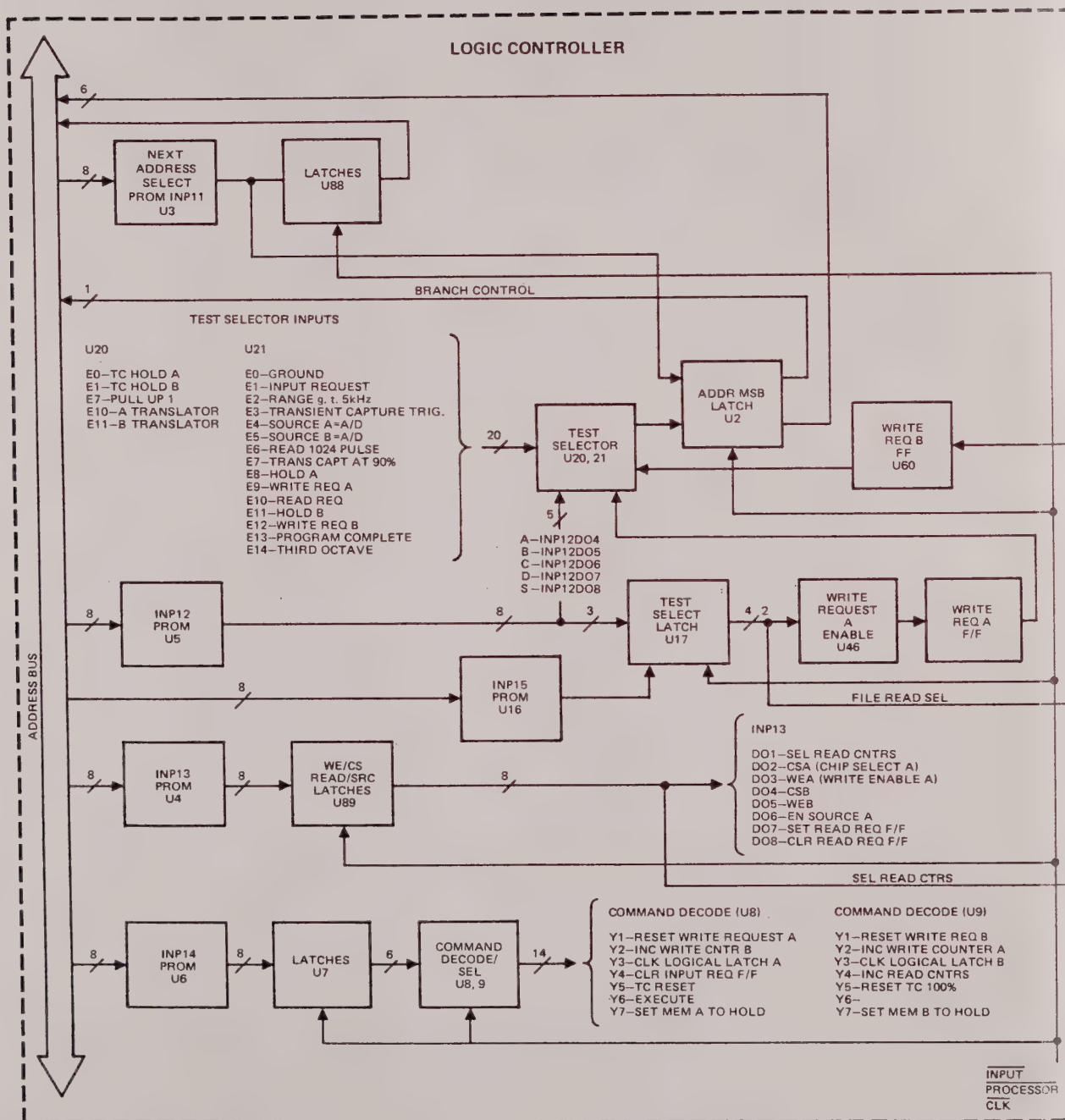
2.5.5 Address Multiplexer

Counter outputs are selected by Address Multiplexers (MUX) A or B and fed to Input Memory A or B address to enable the appropriate storage location for the incoming digital word on the input data bus.

2.5.6 Input Memory

Input Memory A and B are each four chip arrays of 2096 bit static Random Access Memory devices physically organized as 1024 words by 4-bit but connected to accommodate 1024 16-bit words.

Each chip contains input address buffers, row and column decode circuits, input data buffers, data control circuits, output buffers, chip select and write enable inputs.


LOGIC CONTROLLER
ADDRESS BUS
6
8
NEXT ADDRESS SELECT PROM INP11 U3
LATCHES U88
1
BRANCH CONTROL
TEST SELECTOR INPUTS
U20
E0–TC HOLD A
E1–TC HOLD B
E7–PULL UP 1
E10–A TRANSLATOR
E11–B TRANSLATOR
U21
E0–GROUND
E1–INPUT REQUEST
E2–RANGE g. t. 5kHz
E3–TRANSIENT CAPTURE TRIG.
E4–SOURCE A=A/D
E5–SOURCE B=A/D
E6–READ 1024 PULSE
E7–TRANS CAPT AT 90%
E8–HOLD A
E9–WRITE REQ A
E10–READ REQ
E11–HOLD B
E12–WRITE REQ B
E13–PROGRAM COMPLETE
E14–THIRD OCTAVE
20
TEST SELECTOR U20, 21
ADDR MSB LATCH U2
WRITE REQ B FF U60
5
A–INP12DO4
B–INP12DO5
C–INP12DO6
D–INP12DO7
S–INP12DO8
INP12 PROM U5
8
8
3
TEST SELECT LATCH U17
4
2
WRITE REQUEST A ENABLE U46
WRITE REQ A F/F
INP15 PROM U16
FILE READ SEL
INP13 PROM U4
WE/CS READ/SRC LATCHES U89
INP13
DO1–SEL READ CNTRS
DO2–CSA (CHIP SELECT A)
DO3–WEA (WRITE ENABLE A)
DO4–CSB
DO5–WEB
DO6–EN SOURCE A
DO7–SET READ REQ F/F
DO8–CLR READ REQ F/F
SEL READ CTRS
INP14 PROM U6
LATCHES U7
6
COMMAND DECODE/ SEL U8, 9
14
COMMAND DECODE (U8)
Y1–RESET WRITE REQUEST A
Y2–INC WRITE CNTR B
Y3–CLK LOGICAL LATCH A
Y4–CLR INPUT REQ F/F
Y5–TC RESET
Y6–EXECUTE
Y7–SET MEM A TO HOLD
COMMAND DECODE (U9)
Y1–RESET WRITE REQ B
Y2–INC WRITE COUNTER A
Y3–CLK LOGICAL LATCH B
Y4–INC READ CNTRS
Y5–RESET TC 100%
Y6–
Y7–SET MEM B TO HOLD
INPUT PROCESSOR CLK

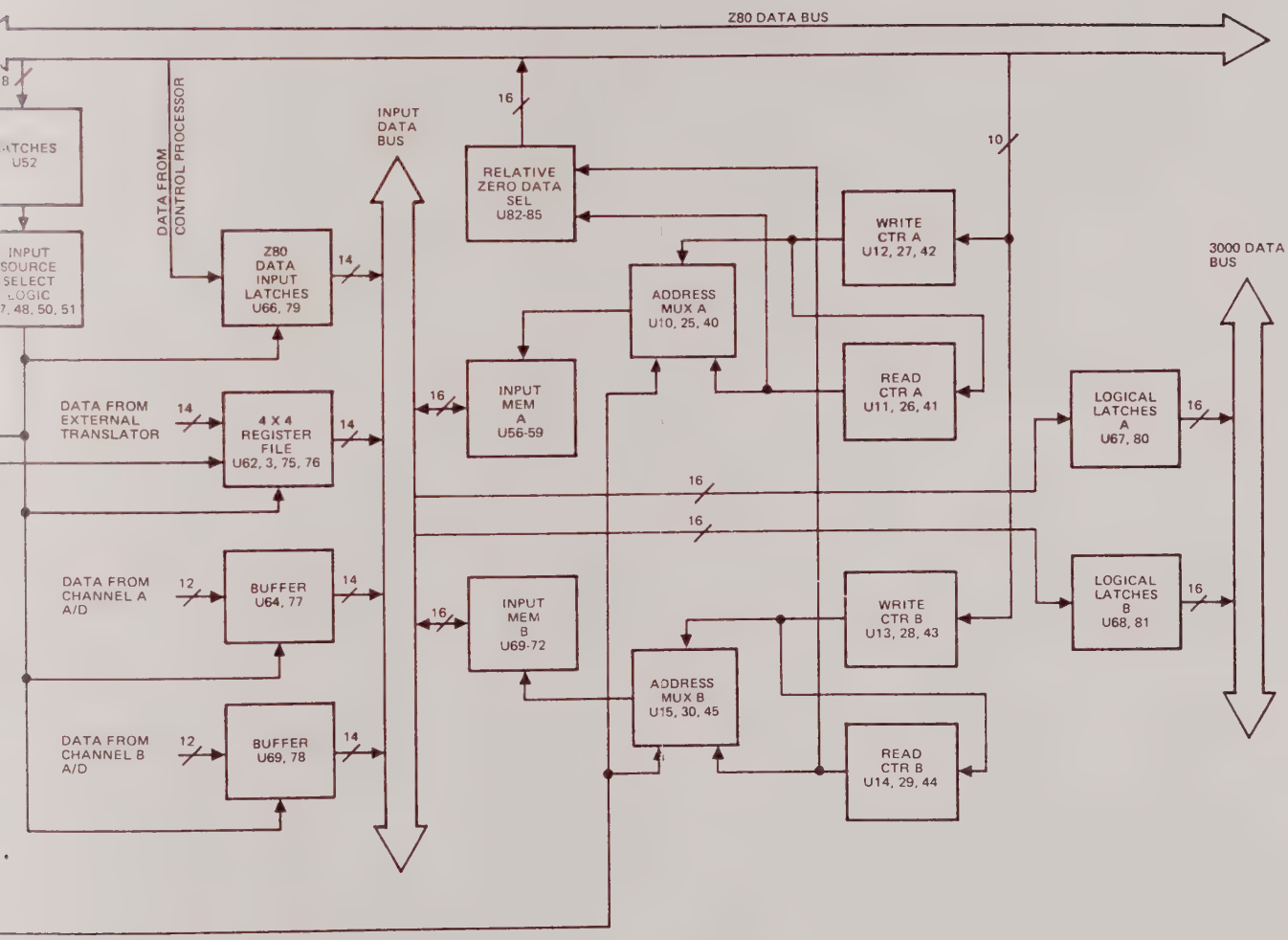

Z80 DATA BUS
INPUT DATA BUS
DATA FROM CONTROL PROCESSOR
RELATIVE ZERO DATA SEL U82-85
WRITE CTR A U12, 27, 42
ADDRESS MUX A U10, 25, 40
READ CTR A U11, 26, 41
INPUT MEM A U56-59
Z80 DATA INPUT LATCHES U66, 79
4 X 4 REGISTER FILE U62, 3, 75, 76
DATA FROM EXTERNAL TRANSLATOR
BUFFER U64, 77
DATA FROM CHANNEL A A/D
BUFFER U69, 78
DATA FROM CHANNEL B A/D
INPUT MEM B U69-72
ADDRESS MUX B U15, 30, 45
WRITE CTR B U13, 28, 43
READ CTR B U14, 29, 44
LOGICAL LATCHES A U67, 80
LOGICAL LATCHES B U68, 81
3000 DATA BUS
16
14
12
10

Figure 2-13. Input Memory Functional Block Diagram

2.5.7 Relative Zero Data Selection

Relative zero data selection is a process by which undesired information is removed from input memory and a function of where the cursor is located. By moving the cursor to the left or right, memory cells are zeroed out by zero data inputs placed on the Z80 data bus and latched to the input bus via Z80 data input buffers.

2.5.8 Input Memory Sequential Operation

The Input Memory PWA operates under the control of address selector U3 (INP11 PROM). INP11 addresses four other PROMs which contain gating instructions and mode controls for all circuitry contained on the Input Memory Assembly.

Figure 2-15 (Input Memory Control Logical Flow Diagram) has been provided to assist the technician in understanding the operational sequence of the input memory.

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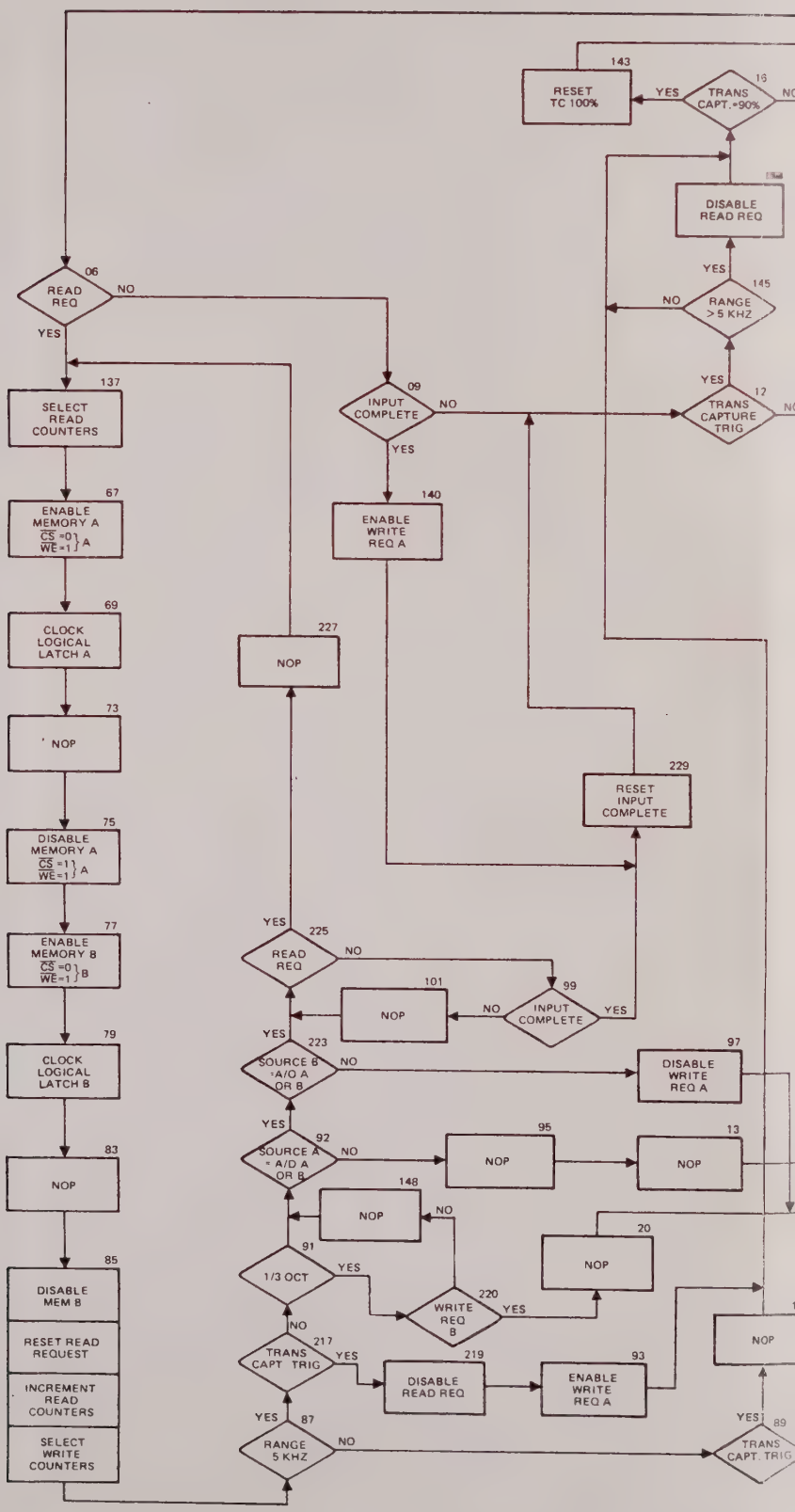

143
RESET TC 100%
YES
16
TRANS CAPT. =90%
NO
DISABLE READ REQ
YES
145
RANGE > 5 KHZ
NO
YES
12
TRANS CAPTURE TRIG
NO
06
READ REQ
NO
YES
137
SELECT READ COUNTERS
09
INPUT COMPLETE
NO
YES
140
ENABLE WRITE REQ A
67
ENABLE MEMORY A
CS =0
WE =1
A
69
CLOCK LOGICAL LATCH A
227
NOP
73
NOP
229
RESET INPUT COMPLETE
75
DISABLE MEMORY A
CS =1
WE =1
A
77
ENABLE MEMORY B
CS =0
WE =1
B
YES
225
READ REQ
NO
99
INPUT COMPLETE
YES
NO
101
NOP
79
CLOCK LOGICAL LATCH B
YES
223
SOURCE B =A/D A OR B
NO
97
DISABLE WRITE REQ A
YES
92
SOURCE A = A/D A OR B
NO
95
NOP
13
NOP
83
NOP
148
NOP
NO
20
NOP
91
1/3 OCT
YES
220
WRITE REQ B
YES
85
DISABLE MEM B
RESET READ REQUEST
INCREMENT READ COUNTERS
SELECT WRITE COUNTERS
NO
217
TRANS CAPT TRIG
YES
219
DISABLE READ REQ
93
ENABLE WRITE REQ A
NOP
YES
87
RANGE 5 KHZ
NO
YES
89
TRANS CAPT. TRIG

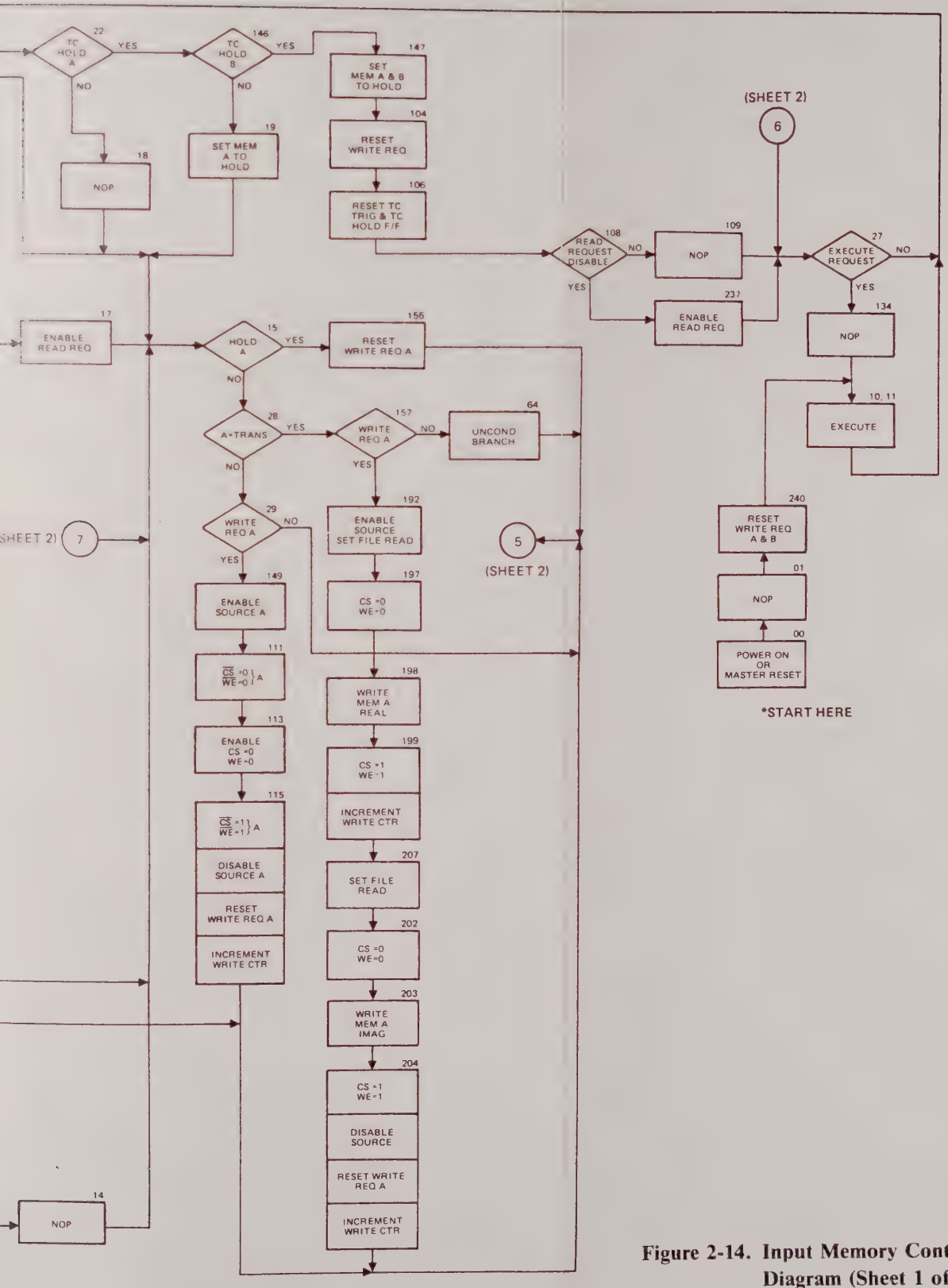
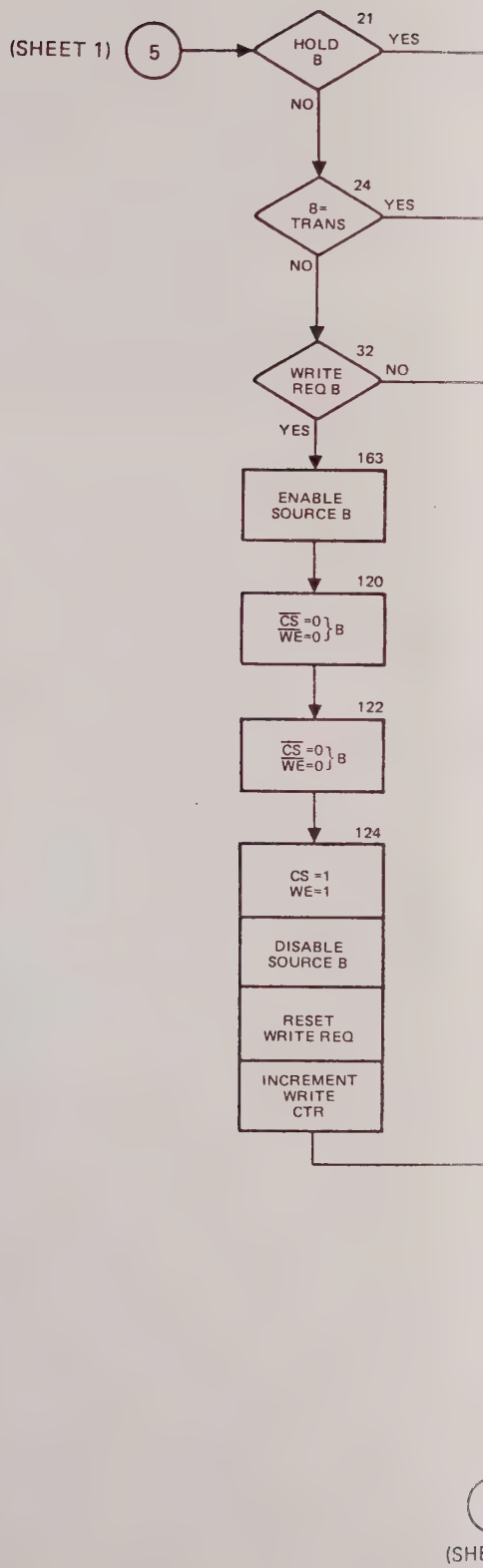


Figure 2-14. Input Memory Control Logic Flow Diagram (Sheet 1 of 2)


(SHEET 1)
5
21
HOLD B
YES
NO
24
B= TRANS
YES
NO
32
WRITE REQ B
NO
YES
163
ENABLE SOURCE B
120
CS =0 WE=0 B
122
CS =0 WE=0 B
124
CS =1 WE=1
DISABLE SOURCE B
RESET WRITE REQ
INCREMENT WRITE CTR
(SHE

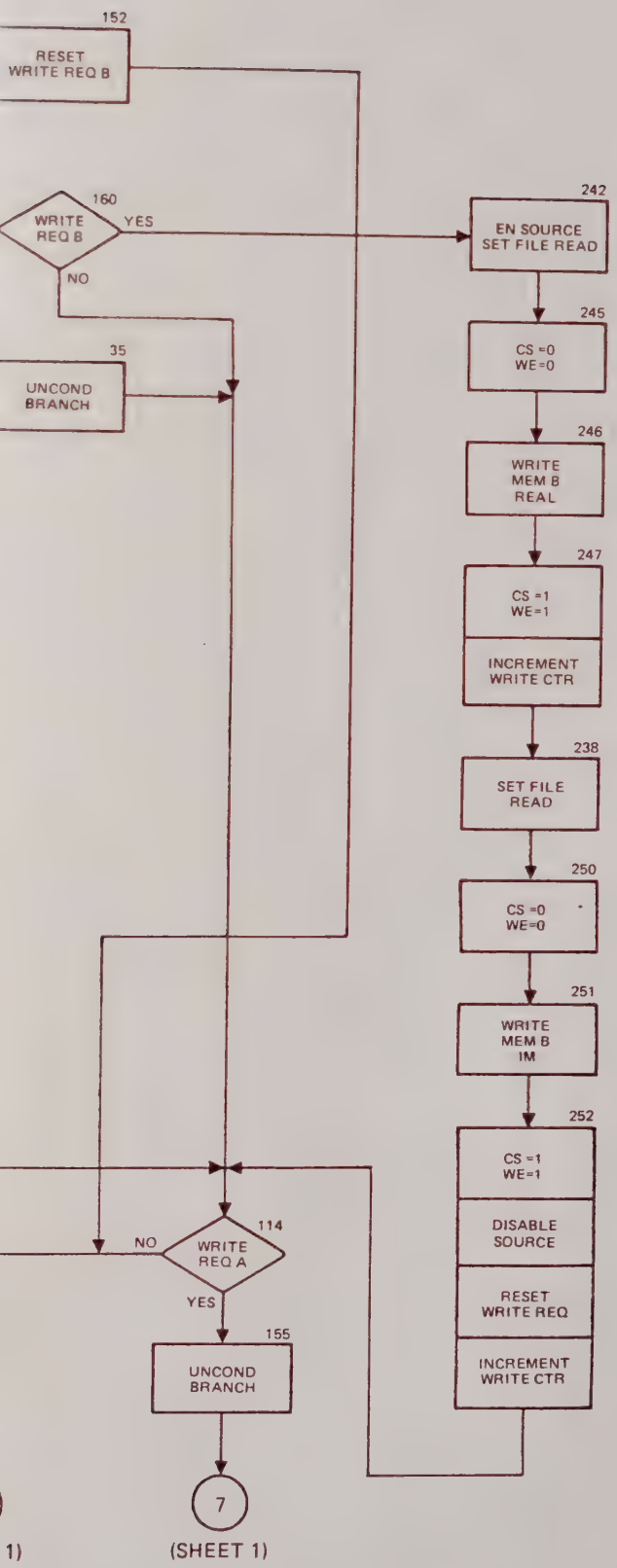


Figure 2-14. Input Memory Control Logic Flow Diagram (Sheet 2 of 2)

2.6 TRANSIENT CAPTURE DETAILED CIRCUIT ANALYSIS

2.6.1 General

The primary functions of Transient Capture circuitry are (1) to determine the source of input signal synchronization and (2) to control the loading of Input Memory based on either the external triggering sources or on parameters (THRESHOLD % and/or DELAY %) entered by the operator.

With the exception of the internal Transient Capture circuitry on the Timing and Control (A5A6) Assembly (shown in Figure 2-15) much of the coordination of Transient Capture functions is accomplished by Input Memory (A5A7) Program Control logic (see Figure 2-14) and the Control Processor (A5A8).

The Detailed Transient Capture circuitry located on the Timing and Control Assembly (A5A6) is found in drawing number 21837000 (sheets 3 and 4). The operational analysis of Transient Capture which follows includes references to the above listed drawings and the simplified block diagram of Figure 2-15.

The Transient Capture functions are implemented using TH % (Threshold Percent) and % Delay (Percent Delay) front-panel touch controls of the Parameters Group in accordance with procedures detailed in the SD375 Dynamic Analyzer II Operator's Manual (P/N 21941600).

Any Threshold Percent inputs between ± 99 percent may be entered by the operator.

Delay % inputs of -100% (one memory period) to +9990% (or 99 memory periods) may be entered in 10% memory period increments.

2.6.2 Transient Capture Circuit Analysis

The Z80 microprocessor addresses the Input section via Address Decode Logic U52, 62, 72 (see Figure 2-15) the Threshold % Latch (U35), the % Delay Latch (U9), the Memory Hold A and B flip-flop (U12), and the Analysis Range Latch (U26). The Threshold % amplitude (triggering level) and the Delay percent (if any) are loaded into their respective latches. The Transient Capture Arm and Time Domain AVG Select bits are latched to the inputs of Trigger Source Select Logic (U33, 25, 29). The Memory Hold A and B flip-flops (U12) are clocked by HOLD A & B and their Q outputs reflect the state of Z80 Data bits D_0 and D_1 which indicate which Input Memory Section (A or B) is to be triggered by the Transient Capture Circuitry.

The A/D A and B signals from Input Signal Conditioners A and B are brought in through Multiplexer (U65, 54) to Transient Capture Comparator (U55, 44).

The Threshold % (Comparator B inputs) is compared (bit by bit) to the A/D input samples (Comparator A inputs) by the Transient Capture Comparator. For positive Threshold % values (TH % LATCH sign bit is low or zero volts), the A > B Comparator output signal must go high (indicating that the A/D A or B signal is larger than the TH %) in order to set the T.C. Trig Pulse Generator (U24).

For negative Threshold % values (sign bits are 1's), the Transient Capture Comparator A < B must go high to set the T.C. Trigger Pulse Generator.

The sign bit (D7) on the Threshold % Latch (U35) and the sign bit of the A/D multiplexer output (U54) are fed to Trigger Selector Strobe circuits (U34). The output pulse from U34 is the Strobe for the T.C. Trigger Selector U45. The only time U45 is strobed is when both sign bits (A/D and Threshold %) are the same.

The Trigger Source Select Logic (U33, 25, 29, 73, Q2 and Q1) accepts the T.C. Trigger pulse and three other trigger source inputs [EXT TRANS CAPT TRIG (pins 1-4), AUTO TRIG (pin 15), and EXT TIME DOMAIN SYNC (pins 12, 13)].

When the EXT TRANS CAPT SEL bit is zero (low), an external trigger must be supplied to J22-13 (Remote Sense and Control Connector). EXT TIME DOMAIN SYNC signals are supplied to J3 on the rear panel.

The Trigger Source Selector (U33) is strobed when either or both inputs to U25 are high (indicating that the Dynamic Analyzer II is armed for transient capture and/or time domain averaging is selected.

The Trigger Source Select Logic pulses the clock input of the Transient Capture Trigger Flip-Flop (U43). With the preset and clear inputs held low by Z80 TR CAPT TRIG and the MEM IN HOLD GATE output, the pulse at the clock input initiates the TRANS CAPT TRIG signal.

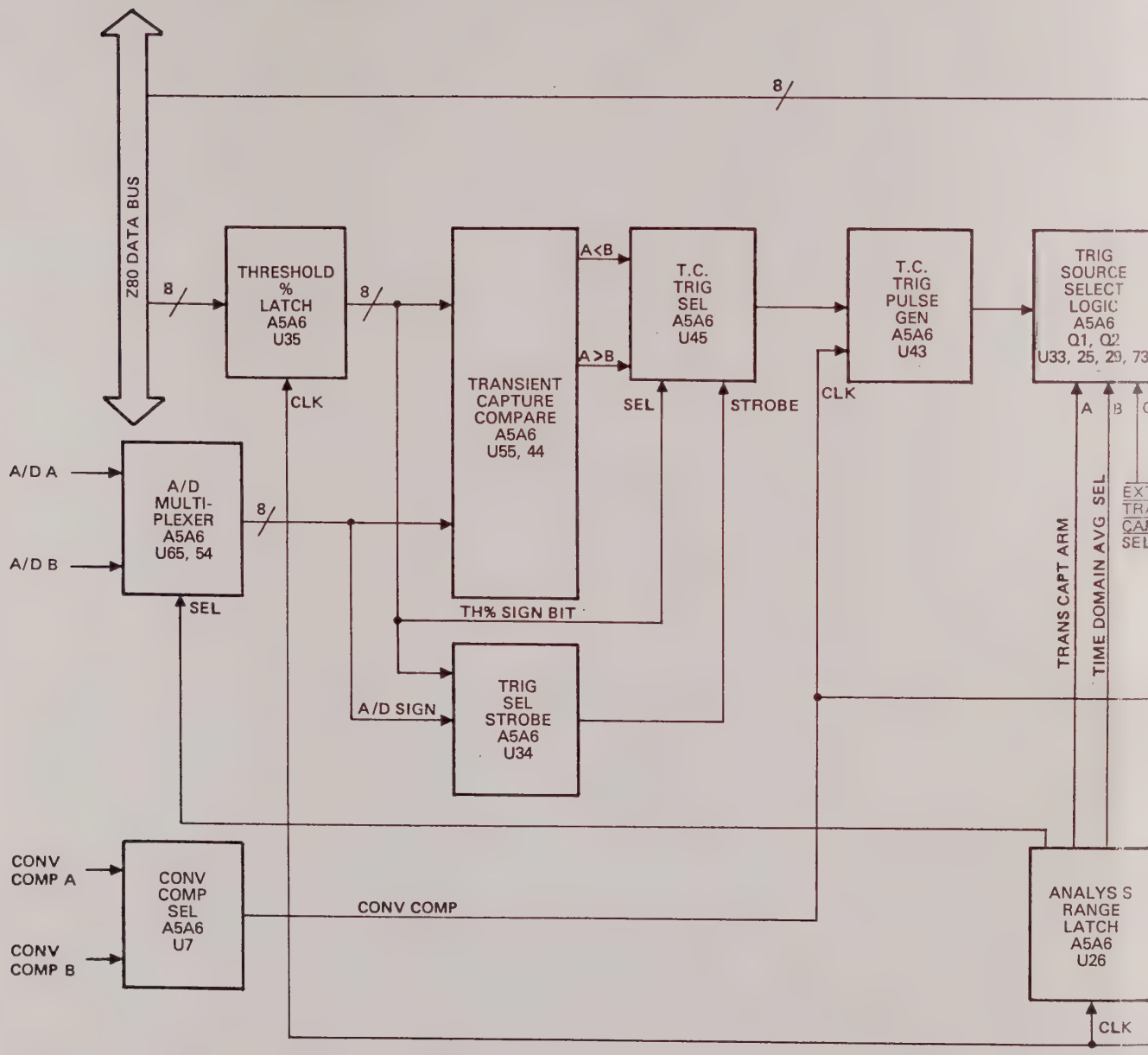
2.6.3 Delay % Circuit Operation

Before the Input Memory can be loaded, any delay inputs entered must be timed out. This is accomplished by feeding TRANS CAPT TRIG (high) to the START/CLOCK Delay Count Down circuit (A5A6 U19). With the high from MEM IN HOLD Gate U30, the START/CLOCK Delay Countdown (U19) produces a negative pulse at the next positive transition of the Conversion Complete Selector (U7) output. This action clocks the LOAD NEXT 100% flip-flop (U5) low. Through LOAD DELAY % Gate U6, The Capture Started signal loads Delay % Countdown Counter (U2, 3, U8) with either the entire delay percent or the first 100% (if the Delay % is greater than 100%).

The T.C. START TRIGGER GENERATOR (A5A6 U24) is triggered by Capture Started. Its output (TRANS CAPT START) is fed to the Control Processor (A5A8) Interrupt Priority Logic. Each time the Input Signal Conditioner (A5A1 or A2) completes an A/D conversion, the Delay % Countdown Counter is decremented. When 90% of the Initial Delay has been processed, the T.C. AT 90% flip-flop (U4). is clocked low.

The Delay % Countdown Counter is loaded again to 100% once it counts down to zero (by LOAD DELAY % GATE U6, U34).

When the entire cycle has been completed and a complete ensembly processed to Input Memory, the Control Processor sends the MASTER RESET to restore initial conditions on the transient capture circuitry. The Transient Capture Trigger flip-flop (U43) is cleared and the T.C. END Delay multivibrator (U24) is triggered. The END Delay trigger (TRANS CAPT END) is fed to Interrupt Priority Logic on the Control Processor (A5A8) Assembly.


280 DATA BUS
8
THRESHOLD % LATCH A5A6 U35
8
CLK
TRANSIENT CAPTURE COMPARE A5A6 U55, 44
A<B
A>B
T.C. TRIG SEL A5A6 U45
SEL
STROBE
T.C. TRIG PULSE GEN A5A6 U43
CLK
TRIG SOURCE SELECT LOGIC A5A6 Q1, Q2 U33, 25, 29, 73
A
B
TRANS CAPT ARM
TIME DOMAIN AVG SEL
A/D A
A/D B
A/D MULTI-PLEXER A5A6 U65, 54
8
SEL
TH% SIGN BIT
A/D SIGN
TRIG SEL STROBE A5A6 U34
CONV COMP A
CONV COMP B
CONV COMP SEL A5A6 U7
CONV COMP
ANALYS S RANGE LATCH A5A6 U26
CLK

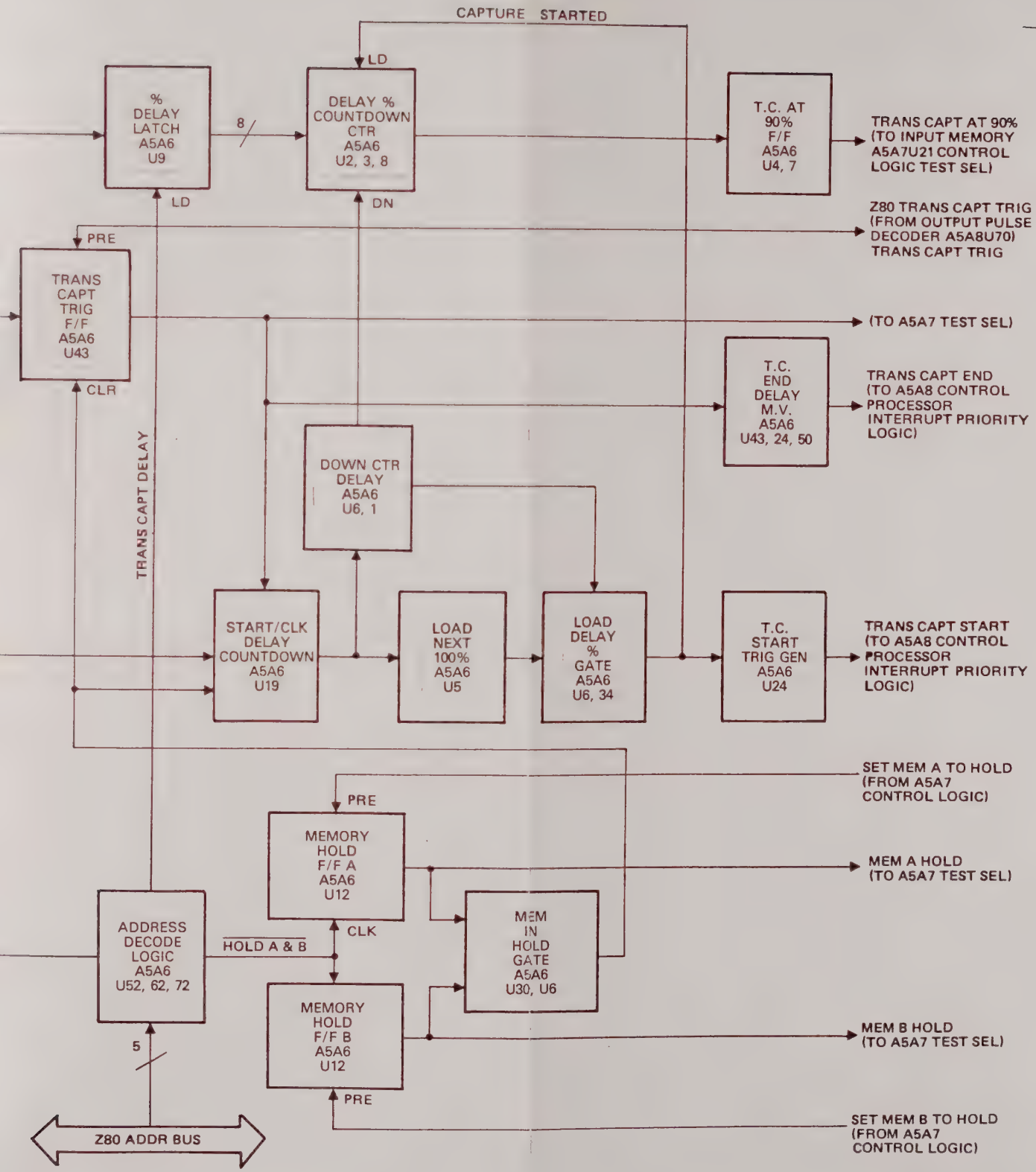

CAPTURE STARTED
LD
% DELAY LATCH A5A6 U9
8
DELAY % COUNTDOWN CTR A5A6 U2, 3, 8
T.C. AT 90% F/F A5A6 U4, 7
TRANS CAPT AT 90% (TO INPUT MEMORY A5A7U21 CONTROL LOGIC TEST SEL)
LD
DN
Z80 TRANS CAPT TRIG (FROM OUTPUT PULSE DECODER A5A8U70) TRANS CAPT TRIG
PRE
TRANS CAPT TRIG F/F A5A6 U43
(TO A5A7 TEST SEL)
CLR
T.C. END DELAY M.V. A5A6 U43, 24, 50
TRANS CAPT END (TO A5A8 CONTROL PROCESSOR INTERRUPT PRIORITY LOGIC)
TRANS CAPT DELAY
DOWN CTR DELAY A5A6 U6, 1
START/CLK DELAY COUNTDOWN A5A6 U19
LOAD NEXT 100% A5A6 U5
LOAD DELAY % GATE A5A6 U6, 34
T.C. START TRIG GEN A5A6 U24
TRANS CAPT START (TO A5A8 CONTROL PROCESSOR INTERRUPT PRIORITY LOGIC)
SET MEM A TO HOLD (FROM A5A7 CONTROL LOGIC)
PRE
MEMORY HOLD F/F A A5A6 U12
MEM A HOLD (TO A5A7 TEST SEL)
ADDRESS DECODE LOGIC A5A6 U52, 62, 72
HOLD A & B
CLK
MEM IN HOLD GATE A5A6 U30, U6
MEMORY HOLD F/F B A5A6 U12
MEM B HOLD (TO A5A7 TEST SEL)
5
PRE
Z80 ADDR BUS
SET MEM B TO HOLD (FROM A5A7 CONTROL LOGIC)

Figure 2-15. Transient Capture Simplified Block Diagram

2.7 PROCESSOR MEMORY DETAILED CIRCUIT DESCRIPTION

2.7.1 General

The primary function of processor memory is to provide storage for the Input Memory data that has been processed by the 3000 CPE. The Processor Memory Assembly (A5A13) includes the following memory arrays: Processor, Refresh, Averager, M2, and Cursor Memories. The Processor Memory Assembly supplies plotter data via the Z80 data bus and the Plotter Data Latch (U78–80). In addition, TV memory data (vertical and cursor) is supplied to the output display circuitry.

2.7.2 Processor Memory Circuit Description

The functional block diagram in Figure 2-16 contains all major circuits of the Processor Memory Assembly. Detailed schematics are located in Volume II of this manual.

2.7.2.1 Addressing the Processor Memory (PM) is accomplished by means of the 16-bit code on the 3000 Address Bus to the Memory Address Drivers (U17), the Chip Select Logic (U52, 53, 70–73) and the X-ADDR MUX (Multiplexer) U34, 50, 51. The high order address bits ($A_{11} \rightarrow A_{15}$) are decoded by the Chip Select Logic to enable the particular array being addressed for read/write operations.

2.7.2.2 The reading and writing to/from the various arrays is accomplished by enabling the Memory Bus Transceiver (U56–59). Data on the 3000 Data Bus is then placed on the Memory Bus to the array being addressed or fed from memory to the 3000 Data Bus.

2.7.3 Refresh Memory Data

To write Refresh Memory data, Processor Memory A or B data is placed on the 3000 Data Bus to the Refresh Memory Data Drivers (U60, 65). Refresh Memory is addressed via the X-ADDR MUX with the X-ADDRESS from Cursor Control Assembly (A5A14) for read operations. Refresh Memory data is simultaneously written to the TV Memory on A5A16. Address inputs are received from the 3000 Address Bus for writing Refresh Memory data.

2.7.3.1 Refresh Memory data is accessed by output display circuitry on the Cursor Control (A5A14), Memory Address (A5A15), and Video Interface Assemblies via TV Vertical Data Selector (U61–63).

2.7.3.2 Plotter Data

Digital plotter data is placed on the Z80 data bus from Plotter Data Latch (U78–80). This data is composed of a horizontal component and a vertical component. The horizontal component is either the X-Address bits from the XADDR MUX or data from the 3000 Data bus via the Refresh Memory Data Drivers. The vertical component of plotter data is either Refresh Memory A or B data.

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To write Refresh Memory data, Processor Memory A or B data is placed on the 3000 Data Bus to the Refresh Memory Data Drivers (U60, 65). Refresh Memory is addressed via the X-ADDR MUX with the X-ADDRESS from Cursor Control Assembly (A5A14) for read operations. Refresh Memory data is simultaneously written to the TV Memory on A5A16. Address inputs are received from the 3000 Address Bus for writing Refresh Memory data.

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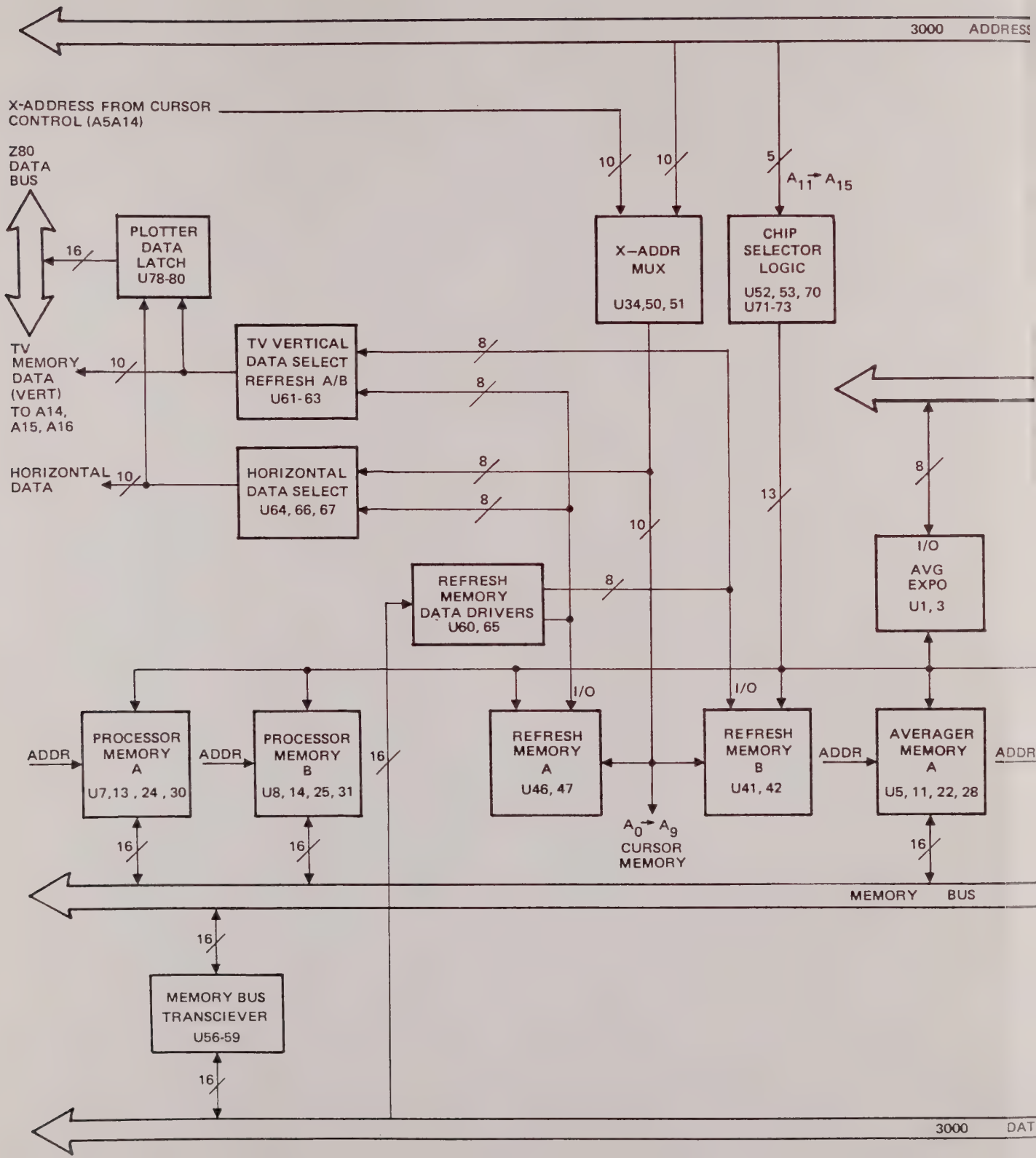
Digital plotter data is placed on the Z80 data bus from Plotter Data Latch (U78–80). This data is composed of a horizontal component and a vertical component. The horizontal component is either the X-Address bits from the XADDR MUX or data from the 3000 Data bus via the Refresh Memory Data Drivers. The vertical component of plotter data is either Refresh Memory A or B data.

(INTENTIONALLY LEFT BLANK)


3000 ADDRESS
X-ADDRESS FROM CURSOR CONTROL (A5A14)
Z80 DATA BUS
16
PLOTTER DATA LATCH U78-80
10
10
5
A11 → A15
X–ADDR MUX U34,50, 51
CHIP SELECTOR LOGIC U52, 53, 70 U71-73
TV MEMORY DATA (VERT) TO A14, A15, A16
10
TV VERTICAL DATA SELECT REFRESH A/B U61-63
8
8
HORIZONTAL DATA
10
HORIZONTAL DATA SELECT U64, 66, 67
8
8
10
13
8
I/O AVG EXPO U1, 3
REFRESH MEMORY DATA DRIVERS U60, 65
8
I/O
I/O
ADDR
PROCESSOR MEMORY A U7,13 , 24 , 30
ADDR
PROCESSOR MEMORY B U8, 14, 25, 31
16
REFRESH MEMORY A U46, 47
REFRESH MEMORY B U41, 42
ADDR
AVERAGER MEMORY A U5, 11, 22, 28
ADDR
16
16
A0 → A9 CURSOR MEMORY
16
MEMORY BUS
16
MEMORY BUS TRANSCIEVER U56-59
16
3000 DAT

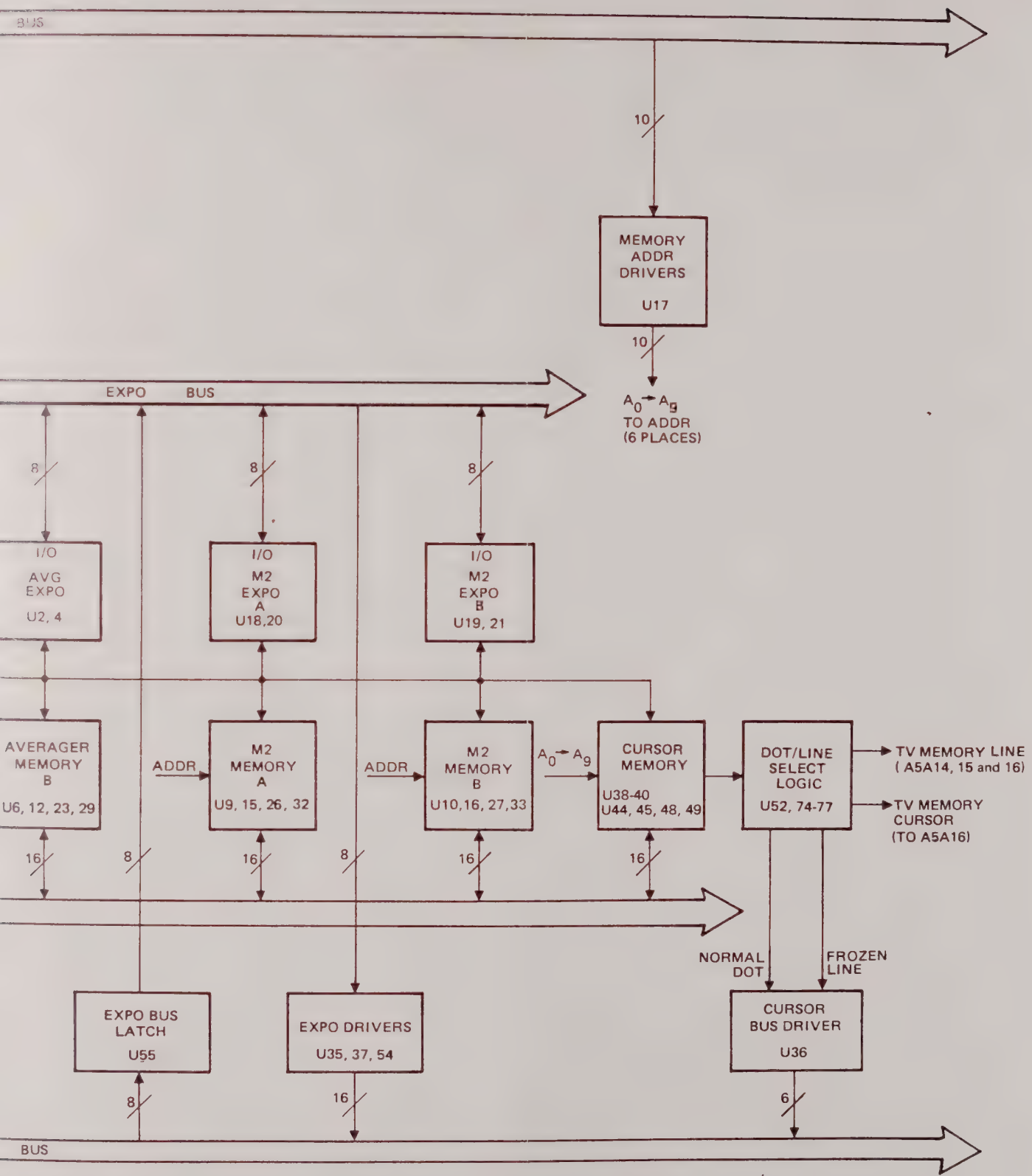


Figure 2-16. Processor Memory (A5A13) Functional Block Diagram

2.8 MICROPROGRAM CONTROL SECTION

2.8.1 General

This section provides the timing and control for controlling the Data Bus and for the processing functions performed by the CPU Section. It contains control PROM's which are capable of providing over 5000 24-bit machine language instructions. Front-panel, Z80 Microprocessor, and the state of various circuits operations throughout the instrument, are monitored in order to control the sequence in which the instructions are fetched from the control PROM's. The Microprogram Control Assembly hardware is contained on the A5A11 printed wiring assembly.

The format of microprogram instruction words is illustrated in Figure 2-17. The three MSB's ($I_{21} \rightarrow I_{23}$) are decoded by the Operation Decoder (U68 on Figure 2-19) as SEL 0 through SEL 5 signals and used internally by the Microprogram Controller for controlling the address generator. The instruction format varies with each program mode.

Basic timing for the Microprogram Control Section is provided by the Phase 1 and Phase 2 clocks from the Program Clock Generator on the A5A6 card.

2.8.2 Microprogram Address Generation

At the heart of the Microprogram Control circuitry is the Address Generator (U40–43). This device controls the sequence in which microinstructions are fetched from control PROMs U4-8, U18-22, U33-37. The Address Generator incorporates four cascaded type SN74S482 4-bit expandable control elements. A complete description of the Expandable Control Element was taken from Texas Instruments Incorporated data sheets and is included in Appendix D.

2.8.2.1 Address Generator Control

The hardware controlling the operation of the Address Generator include the Jump Address Multiplexer (as controlled by the Current Address + 1 gate U56) and the Next State Mode Latch (U44). These circuits select the source of the Address Generator Inputs (see Table 2-1).

2.8.2.2 The Jump Address Multiplexer provides the Carry Input (C_{IN}) to increment the Address Generator. Jump Modes decoded by U56 are anded with the Carry Input (C_i) bit (I_{14} of the microinstruction) and fed through the Jump Address MUX (U27) to the Address Generator. See Table 2-2.

2.8.2.3 Machine State Test Circuitry

Machine State Test circuitry includes the Machine State Test Multiplexer (U58–60), the Next State Mode Selector (U47), and the Next State Mode Latch (U44).

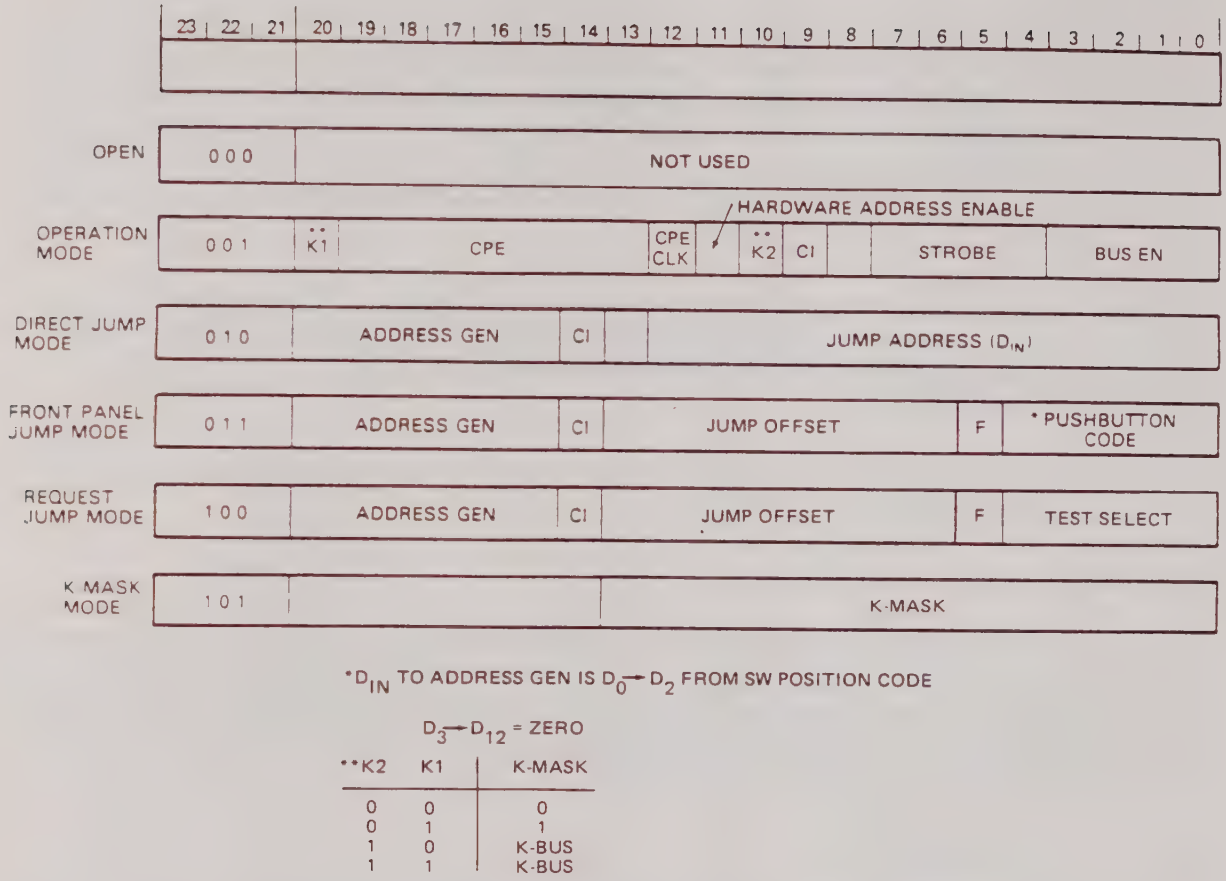
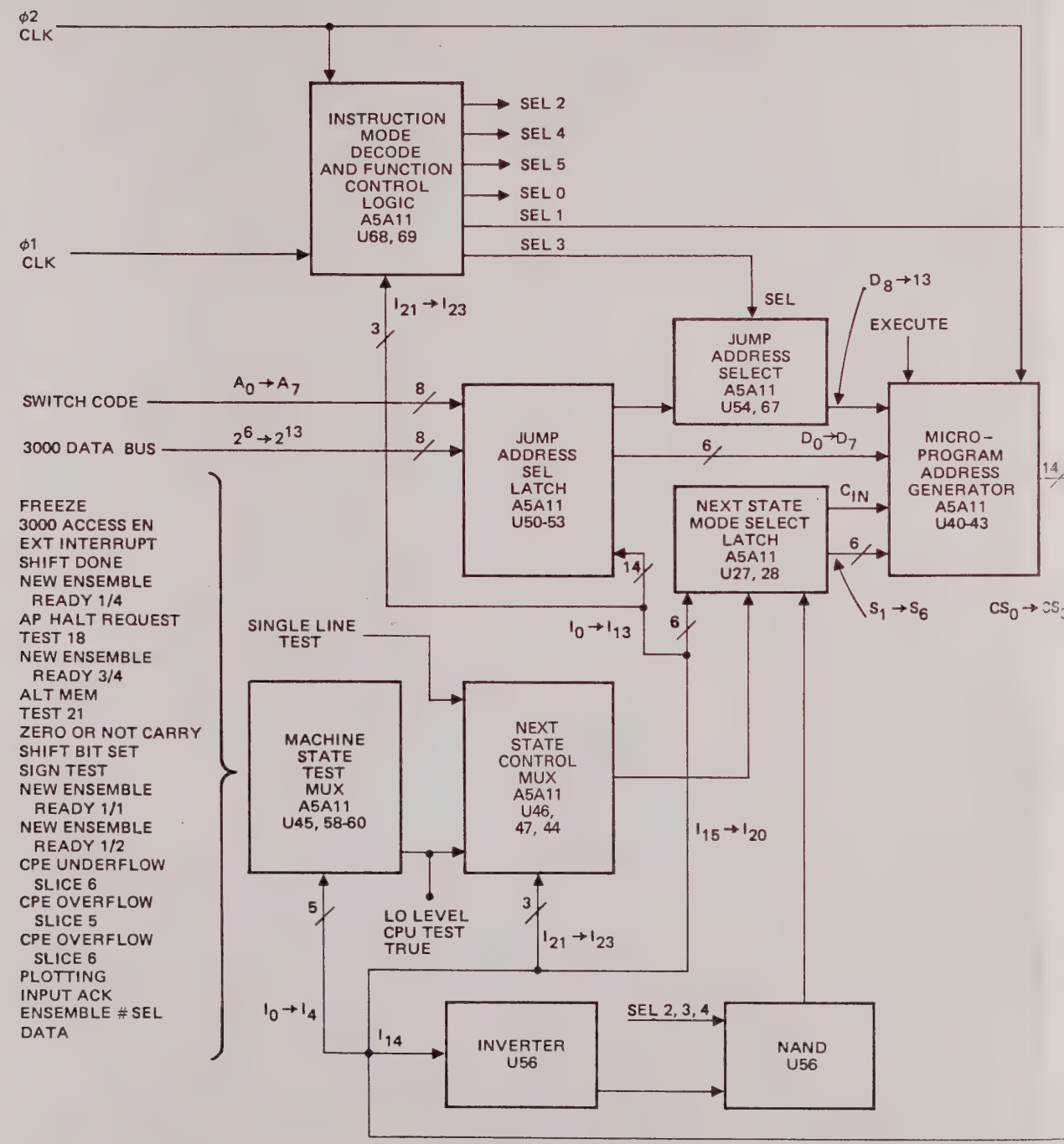


Figure 2-17. Microprogram Instruction Word Format

The machine State Test MUX receives 23 two-state system inputs which are monitored to determine which microinstructions should be accessed when in mode 4 (Request Jump Mode). Microinstruction bits I_0 through I_4 are decoded to select the machine state to be monitored.

In mode 3 the Next State Mode Selector is disabled and the Address Generator accepts the Switch Code and 3000 Data bits via the Jump Address MUX.

The Switch Code can be any of a possible 256 discrete codes which describe front panel touch control selections (that have been made by the operator) as generated on the front panel Interface Assembly (A5A18). The switch codes will result in accessing microinstruction subroutines for the 3000 CPE processes based on operator inputs.


φ2 CLK
φ1 CLK
INSTRUCTION MODE DECODE AND FUNCTION CONTROL LOGIC A5A11 U68, 69
SEL 2
SEL 4
SEL 5
SEL 0
SEL 1
SEL 3
I21 → I23
3
SEL
D8 → 13
EXECUTE
JUMP ADDRESS SELECT A5A11 U54, 67
A0 → A7
SWITCH CODE
8
3000 DATA BUS
26 → 213
8
JUMP ADDRESS SEL LATCH A5A11 U50-53
6
D0 → D7
MICRO-PROGRAM ADDRESS GENERATOR A5A11 U40-43
14
CIN
NEXT STATE MODE SELECT LATCH A5A11 U27, 28
6
S1 → S6
CS0 → CS3
14
I0 → I13
6
SINGLE LINE TEST
FREEZE
3000 ACCESS EN
EXT INTERRUPT
SHIFT DONE
NEW ENSEMBLE READY 1/4
AP HALT REQUEST
TEST 18
NEW ENSEMBLE READY 3/4
ALT MEM
TEST 21
ZERO OR NOT CARRY
SHIFT BIT SET
SIGN TEST
NEW ENSEMBLE READY 1/1
NEW ENSEMBLE READY 1/2
CPE UNDERFLOW SLICE 6
CPE OVERFLOW SLICE 5
CPE OVERFLOW SLICE 6
PLOTTING
INPUT ACK
ENSEMBLE # SEL
DATA
MACHINE STATE TEST MUX A5A11 U45, 58-60
NEXT STATE CONTROL MUX A5A11 U46, 47, 44
I15 → I20
5
LO LEVEL CPU TEST TRUE
3
I21 → I23
I0 → I4
I14
INVERTER U56
SEL 2, 3, 4
NAND U56

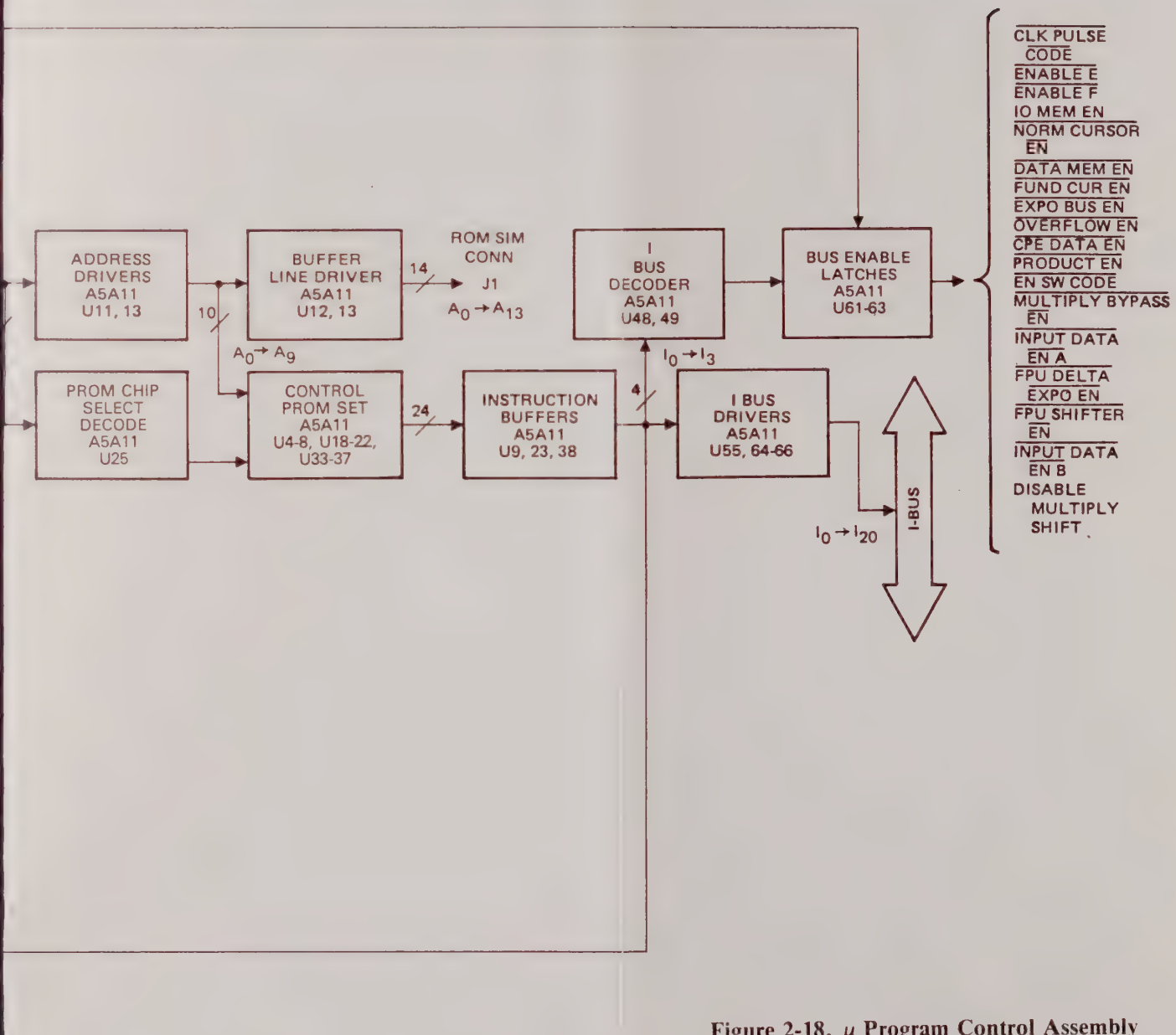


Figure 2-18. μ Program Control Assembly (A5A11) Detailed Block Diagram

Table 2-1. Address Generator Control Selection

Select Code			Single Line Test	Machine State Test	Data Into Address Generator	Address Generator Control							Next Address
I_{23}	I_{22}	I_{21}				S_6	S_5	S_4	S_3	S_2	S_1	C_{IN}	
0	0	0	NA	NA	NA	1	0	0	0	0	1	1	+1
0	0	1	NA	NA	NA	1	0	0	0	0	1	1	+1
0	1	0	NA	NA	I_0 I_{11}	I_{20}	I_{19}	I_{18}	I_{17}	I_{16}	I_{15}	I_{14}	Jump
0	1	1	True	NA	Switch Code	1	0	0	0	0	1	I_{14}	Hold or +1
0	1	1	False	NA	Switch Code	I_{20}	I_{19}	I_{18}	I_{17}	I_{16}	I_{15}	I_{14}	Jump
1	0	0	NA	True	I_6 I_{11}	I_{20}	I_{19}	I_{18}	I_{17}	I_{16}	I_{15}	I_{14}	Jump
1	0	0	NA	False	I_6 I_{11}	1	0	0	0	0	1	I_{14}	Hold or +1
1	0	1	NA	NA	NA	1	0	0	0	0	1	1	+1

Table 2-2. Jump Address Decoding

Address Generator Control							Jump Address
S_6	S_5	S_4	S_3	S_2	S_1	C_{IN}	
0	0	X	X	X	X	X	Data In
0	1	X	X	X	X	X	From Address Generator Stack
1	0	X	X	0	0	0	Present Address + Data In
1	0	X	X	0	0	1	Present Address + Data In + 1
1	0	X	X	0	1	0	Hold Present Address
1	0	X	X	0	1	1	Next Sequential Address
1	0	X	X	1	0	0	Data In
1	0	X	X	1	0	1	Data In + 1
1	0	X	X	1	1	0	Address 0000
1	0	X	X	1	1	1	Address 0001
1	1	X	X	X	X	X	Hold Present Address

In mode 2, the address input to the Address Generator is a 14-bit Jump Address from the microprogram instruction.

Next State Mode Selector supplies source bits to the Address Generator for modes 2 through 4. These source bits are S1 through S6 and are bits I_{15} through I_{20} of the microinstruction or the current Address + 1 Code (100001).

The output of the Next State Control Mux is determined by the mode control bits (I_{21}, I_{22}, and I_{23}) of the microinstruction and is, therefore, dependent upon the selected mode as follows:

a. For modes 0, 1, or 5, the output of Next State Control Mux is always high.

b. For mode 2, the output of the Next State Control Mux is always low.

c. For mode 3, the output of the Next State Control Mux is dependent upon the result of a test of the Single Line Test Logic which provides a high level when a test is true.

d. For mode 4, the output of the Next State Control Mux is dependent upon the result of a test of the Machine State Test Mux which provides a low level when a test is true.

2.8.3 K-Mask Mode (Mode 5)

When the K-Mask mode is decoded, bits I_0 through I_{15} of the microinstruction word are fed to the Arithmetic Processor's 3000 CPE as the K-Bus input and is retained until a new K-Mask is loaded.

2.8.4 Bus Enables

The Operation Mode Decoder (U48, 49) decodes bits $I_0 \rightarrow I_3$ to provide bus controls (levels) as required to gate data to and from the Arithmetic Processor (3000 CPE).

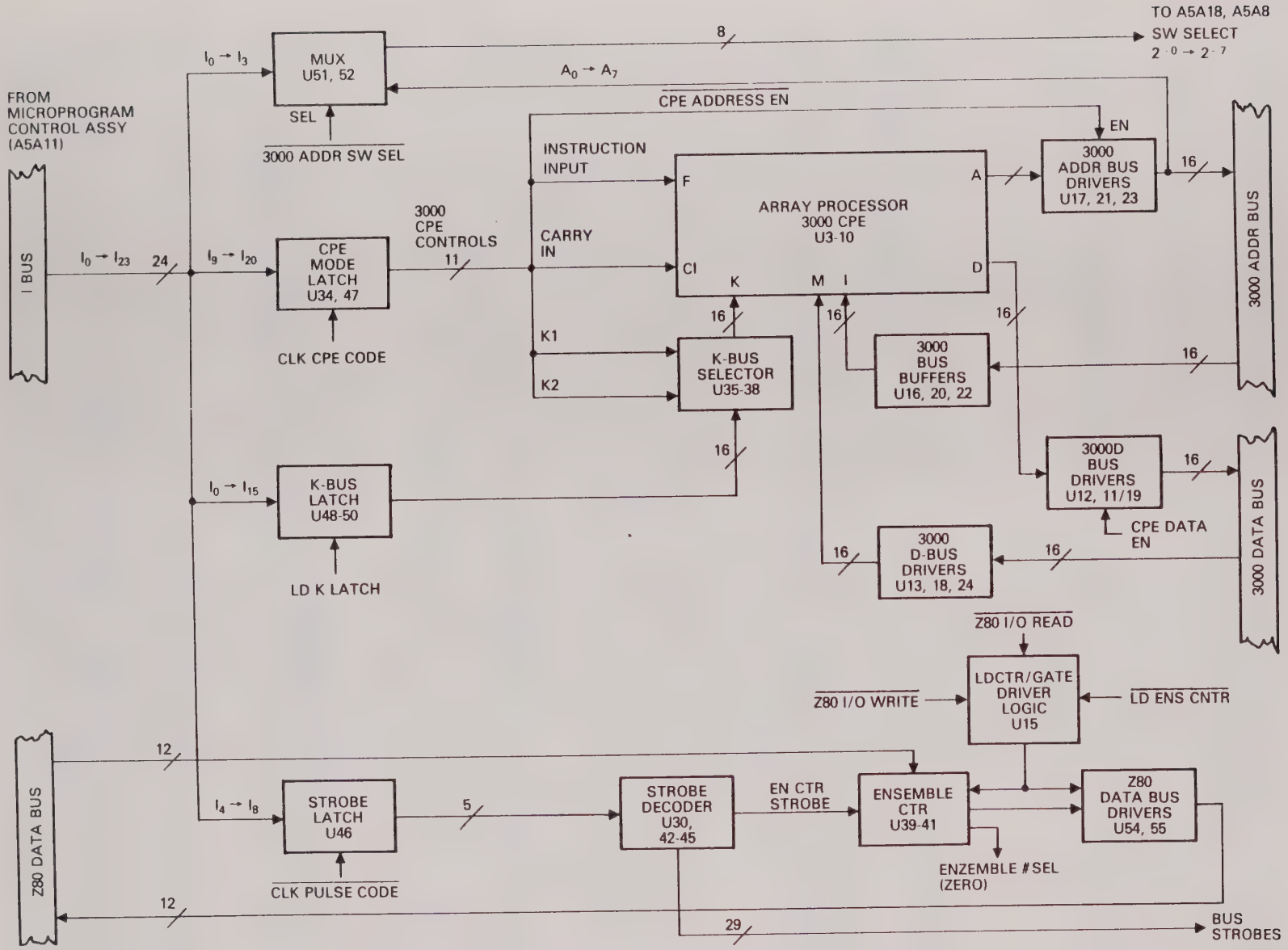


Figure 2-19. Arithmetic Processor (A5A12) Functional Block Diagram

2.9 CENTRAL PROCESSING UNIT (CPU)

2.9.1 General

The CPU is comprised of circuitry on several different PWAs as outlined below.

Arithmetic Processor	A4A12
Multiplier	A5A10
Processor Memory	A5A13
Averager Memory	A5A13
Memory Address	A5A15

The Memory Address PWA (A5A15) contains all circuitry required to address appropriate data contained in the Processor Memory and required by the Arithmetic Processor in executing arithmetic and logical functions on the input data as directed by microinstructions it receives from the Microprogram Control PWA (A5A11). The Memory Address PWA also contains SINE, COSINE, SQUARE ROOT, LOG X, WEIGHTING, DIVIDE/TANGENT, and special function PROMs which contain required data values used by the CPU for arithmetic functions.

The Processor Memory and Averager Memory (A5A13), and the Memory Address Circuitry are discussed in Sections 2.6 and 2.10, respectively. This discussion will be limited primarily to the functions of the Arithmetic Processor. The Multiplier Assembly (A5A10) is discussed in Section 2.11.

2.9.2 Arithmetic Processor

The Arithmetic Processor is commonly referred to as the 3000 CPE. It basically consists of eight 2-bit slice (type 3002) central processing elements which are cascaded to form a 16-bit array processor. Excerpts from Signetics Corporation data sheets of the N3002 CPE are contained in Appendix C to facilitate the technician's understanding of the Arithmetic Processor's operation.

All Arithmetic Processor (see Figure 2-19) operations are controlled by the microprogram Control Instructions it receives from the A5A11 assembly.

Transfer of data and address information to and from the 3000 CPE is accomplished via the 3000 Data Bus and the 3000 Address Bus respectively.

The 7-bit CPE code from the Microprogram Control Assembly and the K-MASK (associated with mode 5 microprogram instructions) are employed to direct and control the operations of the 3000 CPE.

The mode 1 CPE Code (microprogram instruction bits $I_{13} \rightarrow I_{19}$) is fed to the F (function) input of the 3000 CPE array and are described in Appendix C.

K-Mask data is employed as outlined in Appendix C and is selected for input to the 3000 CPE array from one of two sources by U35 through 38. If the K_2 bit (I_{10}) is high (logical "1"), K-Bus data is the 16-bit code ($I_0 \rightarrow I_{15}$) from the K-Bus Latch (U48-50). When the K_2 bit is low, the status of the K_1 bit (I_{20}) is selected as the 16-bit K-Mask to the 3000 CPE array. With K_2 and K_1 both low, the 16-bit K-Mask is all logical zeros. With K_2 low and K_1 high, all K-Mask bits are logic ones.

The 3000 CPE array processor employs the phase 1 and 2 clock pulses. The phase 1 (Φ1 clock) is used to clock the array processor as gated by the CPE CLK CONTROL signal.

Figure 2-19 is the functional block diagram about which the following description of the 3000 CPE is developed.

The instruction word from Microprogram Control (bits 5 through 9) is fed through Strobe Latch U46 to the Strobe Decoder (U42–45). Bus Strobes are generated to initiate/terminate various operations around the CPU.

2.9.3 Ensemble Counter

AVG N data on the Z80 Data Bus is loaded into the Ensemble Counter (U39-41) by the LD ENS CNTR strobe or the Z80 I/O WRITE signal from the Control Processor (A5A8) Address Logic Decoder and Z80 Control Logic respectively.

Under Microprogram Control, the ensemble counter is clocked by the ENS CTR STROBE after each average is computed by the 3000 CPE. The Ensemble Counter is counted down. When it reaches zero (as detected by U29) the ENSEMBLE # SEL signal is generated and fed to Microprogram Control (Machine State Test MUX) to terminate the strobe to the counter and stop the ensemble averaging cycle.

2.9.4 Switch Select

Switch Select codes are generated by the CPU (in mode 3). Operator switch selections are read from the MAIL BOX RAM on the front panel Interface Assembly (A5A18) as 4-bit codes. They are placed on the 3000 Address Bus and selected by the Switch Select MUX (U51, 52) for input to the Control Processor as SW SEL $2^0 \rightarrow 2^{-7}$ (8-bits).

The alternate Switch Select code is formed by microprogram instruction bits $I_0 \rightarrow I_3$ which are placed on the B inputs to the Switch Select (MUX).

2.10 MEMORY ADDRESS DETAILED CIRCUIT ANALYSIS

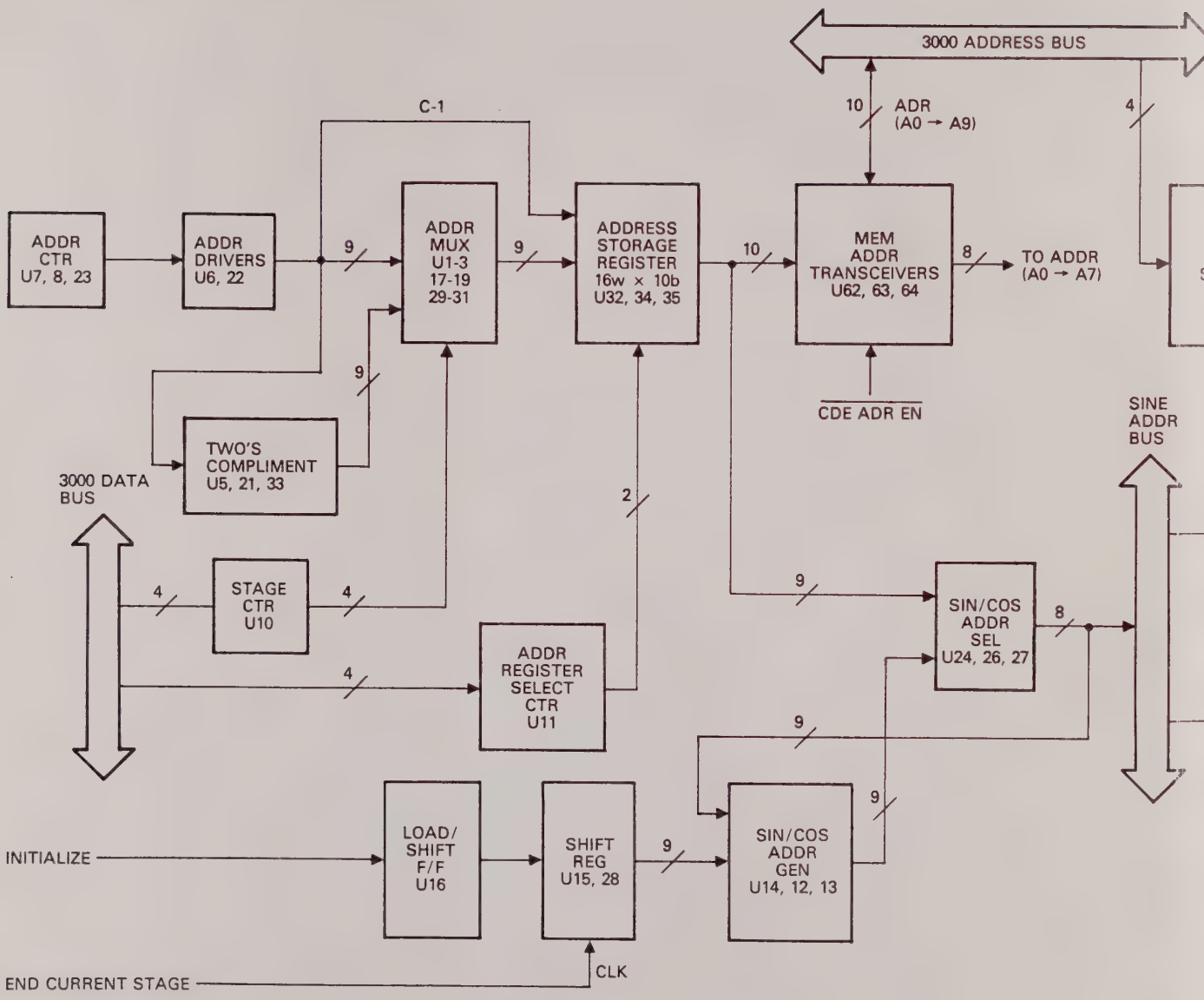
2.10.1 General

The Memory Address circuitry is contained on the A5A15 printed circuit board. Figure 2-20 is a functional block diagram of the Memory Address PWA. Detailed schematics are contained in Volume II drawings (Part Number 21013100).

2.10.1.1 Memory Address Concepts

The Memory Address circuitry primarily functions to generate addresses and address sequences needed by the 3000 CPE for the accessing of processor memory data used in the "butterfly" computations of the Fast Fourier Transform (FFT). The memory address PWA also generate appropriate sine and cosine values required by the 3000 CPE for the FFT operation. Numerous other constants required by the 3000 CPE are accessed from memory and placed on the 3000 data bus to the 3000 CPE. These include weighting, square root, LOG X, and Divide/Tangent constants.

The SD375 employs a ten-stage 16-point algorithm for its Fast Fourier Transform. The hardware used to perform the complexed addressing scheme required to access the sine/cosine constants and processor memory data is accomplished by the circuits illustrated in Figure 2-20 utilizing inputs from the array processor (A5A12). These signals include INITIALIZE, CAC CLOCK, LD ADDR SEL CTR, CLK ADR RAM SEL REGISTER, and END CURRENT STAGE. The Microprogram Control Assembly supplies the EXECUTE and CPE ADR EN signals.


3000 ADDRESS BUS
10
ADR
(A0 → A9)
4
C-1
ADDR
CTR
U7, 8, 23
ADDR
DRIVERS
U6, 22
9
ADDR
MUX
U1-3
17-19
29-31
9
ADDRESS
STORAGE
REGISTER
16w × 10b
U32, 34, 35
10
MEM
ADDR
TRANSCEIVERS
U62, 63, 64
8
TO ADDR
(A0 → A7)
CDE ADR EN
SINE
ADDR
BUS
9
TWO'S
COMPLIMENT
U5, 21, 33
3000 DATA
BUS
2
4
STAGE
CTR
U10
4
4
ADDR
REGISTER
SELECT
CTR
U11
9
SIN/COS
ADDR
SEL
U24, 26, 27
8
9
INITIALIZE
LOAD/
SHIFT
F/F
U16
SHIFT
REG
U15, 28
9
SIN/COS
ADDR
GEN
U14, 12, 13
9
END CURRENT STAGE
CLK

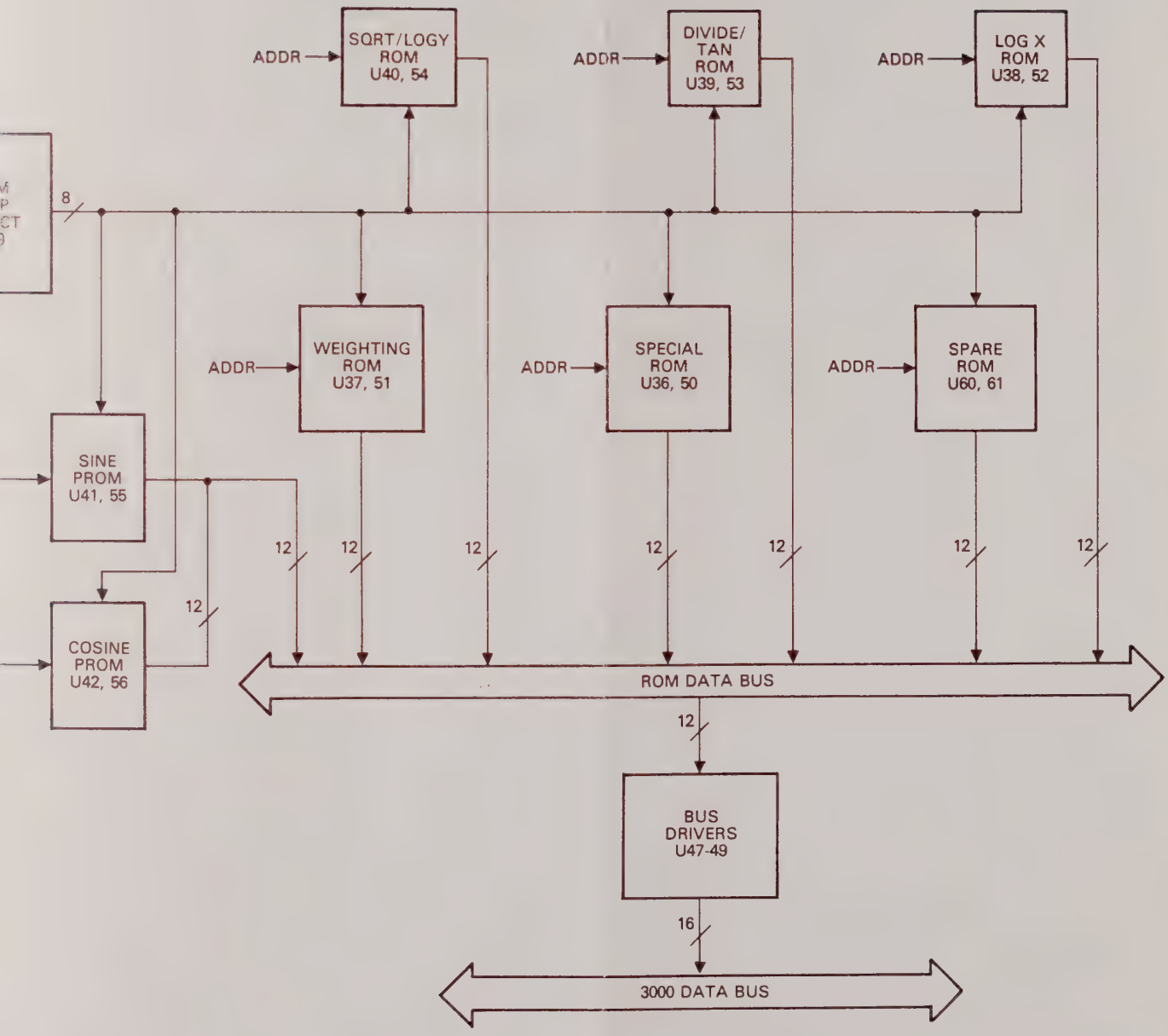


Figure 2-20. Memory Address Assembly (A5A15) Functional Block Diagram

2.10.2 Address Generation

Initial conditions are established by INITIALIZE and EXECUTE. These signals clear the Load/Shift flip-flop (U16) and the Shift Register (U15, 28). The Address Counter (U7, 8, 23) is also cleared. When clocked by CAC CLOCK, the Address Counter's 9-bit output is fed through Drivers (U6, 22) to the Address Multiplexer (MUX U1, 2, 3, 17, 18, 19, 29, 30, 31) and the two's complimentor (U5, 21, 33). The Two's-Complimentor counts down from 1022 while the Address Counter is incremented from 0 to 1023. In this manner, the address scheme required to access the real and imaginary components (of the complexed data word stored in the Processor Memory) for the butterfly. The Address Counter's count, its compliment, and the True 2's compliment are fed to the Address MUX. The Address MUX (U1-3, 17-19, 29-31) supplies the 9-bit address sequence for each of the 16 points required based on inputs from the Stage Counter (U10).

2.10.2.1 Stage Counter and Address Register Select Counter

The Stage Counter (U10) is loaded to the *initial* stage from the 3000 Data Bus by LD ADDR SEL CTR and is incremented by the Central Address Counter (CAC) Clock signal from the 3000 CPE. The 4-bit count in the Stage Counter selects appropriate bits from the Address MUX to form address words required for the given point of the butterfly.

The Address Register Select Counter (U11) is loaded with the 2^{-10} through 2^{-15} bits from the 3000 Data Bus. It is then incremented by the CLK ADR RAM SEL REGISTER strobe from the 3000 CPE to load the four (4) address locations of data in the Processor Memory into the Address Storage Register (U32, 34, 35). The counter (U11) is again used to read the contents of the Address Storage Register when the CPE ADR EN signal is received from Microprogram Control.

The read signal (CPE ADR EN) also places the all four Address Storage Register words on the 3000 Address Bus via the Memory Address Transceivers and (as selected by the ROM Chip Selector U59) to the ROM containing other constants required by the 3000 CPE.

2.10.3 Sine/Cosine Generation

2.10.3.1 The CPE ADR EN signal (when low) results in selecting Address Storage Register (U32, 34, 35) address words. When high, the SIN/COS Address Generator (U14, 12, 13) bits are selected. The negative transition of the LD SIN ADR REG signal places the sine or cosine address word on the output of the Sine/Cosine Address Selector and to the Sine and Cosine PROMS (U41, 42, 55, 56). The nine bits on the Sine/Cosine bus are fed also to the Sine/Cosine Address Generator in order to generate addresses for the other Sine/Cosine values required for point computations of the FFT.

The contents of the Shift Register (U15, 28) is summed with the first address word to appear on the Sine/Cosine Address Selector's output. This sum represents the second value (Sine or Cosine) needed and is clocked to the SIN/COS Address Selector output.

2.11 MULTIPLIER

2.11.1 General

The Multiplier is essentially an extension of the Arithmetic Processor (A5A12) PWA which operates under Microprogram Control to perform rapid two's complement multiplication and normalization of data on the 3000 Data Bus and then return the results to the Data Bus for storage or further processing within the CPU. Figure 2-21 is a functional block diagram of the Multiplier PWA.

2.11.2 Detailed Circuit Analysis

The Multiplier employs eight 93S43 devices in an array capable of producing a partial product. Floating Point Unit circuitry is also incorporated to perform normalization, and denormalization of the exponent of 16-bit binary coded numerical data.

Calculations involving constants (e.e., weighting factors) are performed under Microprogram Control by placing the appropriate data in the Multiplicand Register (U48, 53) via the 3000 Data Bus and Drivers (U35, 36). The LOAD MULT #1 signal is employed to latch the data in the Multiplicand Register. The appropriate weighting factor (from PROM A5A15 U37, 51) is selected and (with the LOAD SHIFT REGISTER signal) is loaded into the Multiplier Shift Register (U19, 21, 25, 27).

2.11.2.1 Multiplication

The multiplication of the weighting factor and the data is accomplished in the Multiplier (U46, 47 and U49-52, U54, U55) as controlled by the MULTIPLY CLOCK signal and the 16-bit resultant partial product is simultaneously clocked into the Partial Product Register (U62, 67 on drawing 21040500 Sheet 4).

2.11.2.2 Bus Gating

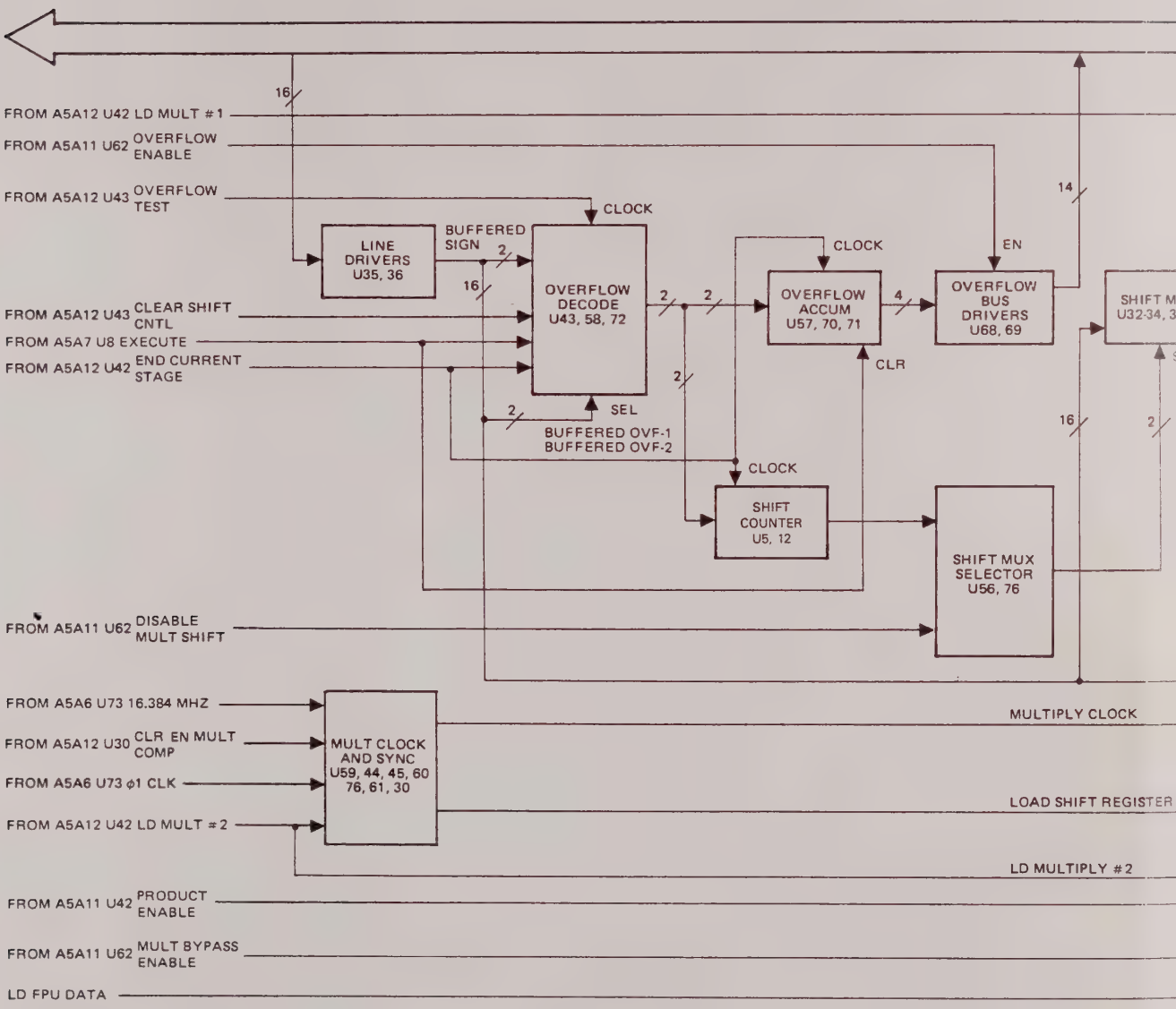
The Partial Product in the Partial Product Register is gated to the 3000 Data Bus through the Partial Product Bus Drivers (U64, 65) when the PRODUCT EN signal is received from the Microprogram Control Assembly (A5A11).

When no multiplication is required, the contents of the Multiplicand Register is bypassed to the Multiplier and is placed on the 3000 Data Bus through the Multiply Bypass (U63, 66) drivers.

2.11.3 Overflow

When the multiply operation is completed, any overflow which has occurred (MULTIPLY 2^{-14}) is fed to the array processor (A5A12) as a shift register input and input to the Carry Look-ahead Generator (A5A12 U2) as CIS0.

During the arithmetic operations of the "butterfly", overflow and current stage data from previous computations is fed the overflow circuits Overflow Decode (U43, 58, 72), Overflow Accumulator (U57, 70, 71), Shift Counter (U5, 12), and the Shift MUX Selector (U56, 76). These circuits function to provide a shift of data placed in the Shift Multiplexer (U32–34, 37–40) and thereby eliminate any resultant overflow from subsequent Multiplier partial products.


FROM A5A12 U42 LD MULT #1
FROM A5A11 U62 OVERFLOW ENABLE
FROM A5A12 U43 OVERFLOW TEST
FROM A5A12 U43 CLEAR SHIFT CNTL
FROM A5A7 U8 EXECUTE
FROM A5A12 U42 END CURRENT STAGE
FROM A5A11 U62 DISABLE MULT SHIFT
FROM A5A6 U73 16.384 MHZ
FROM A5A12 U30 CLR EN MULT COMP
FROM A5A6 U73 ϕ1 CLK
FROM A5A12 U42 LD MULT #2
FROM A5A11 U42 PRODUCT ENABLE
FROM A5A11 U62 MULT BYPASS ENABLE
LD FPU DATA
16
LINE DRIVERS U35, 36
BUFFERED SIGN
2
16
CLOCK
OVERFLOW DECODE U43, 58, 72
2
2
SEL
BUFFERED OVF-1
BUFFERED OVF-2
CLOCK
OVERFLOW ACCUM U57, 70, 71
4
CLR
EN
OVERFLOW BUS DRIVERS U68, 69
14
SHIFT M U32-34, 3
16
2
CLOCK
SHIFT COUNTER U5, 12
SHIFT MUX SELECTOR U56, 76
MULT CLOCK AND SYNC U59, 44, 45, 60 76, 61, 30
MULTIPLY CLOCK
LOAD SHIFT REGISTER
LD MULTIPLY #2

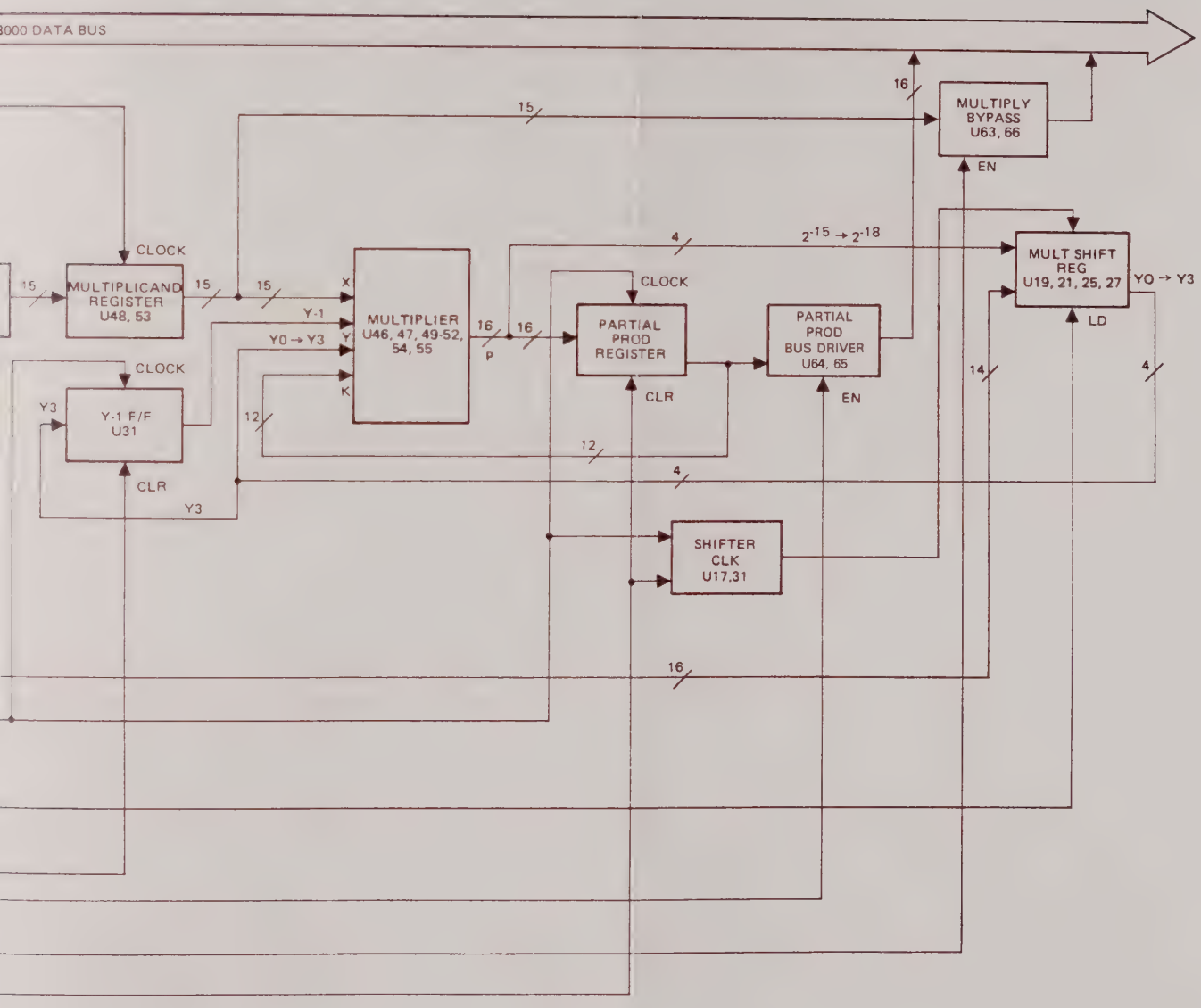


Figure 2-21. Multiplier Functional Block Diagram (P/O A5A10)

2.11.4 FPU Circuit Analysis

2.11.4.1 General Description

The circuitry illustrated in Figure 2-22 is also part of the Multiplier Assembly (A5A10) and is employed to provide normalization and denormalization of CPU data. The detailed schematics appear in Volume II as drawing number 21040500 (Sheet 5).

2.11.4.2 Normalization

Initial conditions are established by MASTER RESET and the LD FPU DATA signal which is fed to U17 to set the state of the sign bit at its output. The state of the 2^{-1} bit is examined by the LEFT/RIGHT/SHIFT DONE Logic to determine if a shift of the data on the Buffered 3000 D-Bus is required to place the MSB of the data in the 2^{-1} bit location. The actual number of bit shifts required is read from the 3000 Data Bus (bits 2^{-10} through 2^{-13}) and latched into the Exponent Input Register (U28) by the LD FPU # SHIFTS signal. The bit organization of the FPU (Floating Point Unit) data is illustrated in Figure 2-24.

If the $2^{1} = 0$, a shift is generated to place the Shifter (U18, 20, 24, 26) output data word in the form $1XXX_{(H)}$. This places the binary point to the left of the MSB.

2.11.4.3 Shifter

The Shifter (A5A10 U18, 20, 24, 26) is comprised of a four-chip array of type SN74S194N Universal Shift Registers in order to handle the 16-bit data input. The Shifter is configured to Load, Shift Right, Shift Left, or do nothing to the data as dictated by mode inputs (S1, S0) it receives from Left/Right/Shift Done Logic (U3, 4, 30) and Stop Logic (U9).

Table 2-4 describes the operations performed by the Shifter on input data.

2.11.5 FPU Operation (NORMALIZE)

The LD FPU DATA signal places a low level at NAND GATES U4 (pins 10 and 13) to drive their outputs high. These two outputs are fed to the mode inputs (S0, S1) of the 16-bit Shifter (U18, 20, 24, 26).

The LD FPU DATA signal also presets U31–Q5 (High) to enable the 8.192 MHz clock pulses. The 8 MHz clock will load the FPU Data into the Shifter.

A hard wired plus two (+2) is loaded from the Exponent Input Selector (U13) to the Exponent Counter (U5, U12).

From the Shift Stop Logic, a high level at U17–Q9 is placed on exclusive or gate U2–9. The 2^{1} bit is fed from the Shifter U18-14 to U2-10.

If 2^{1} is a 1 (High) a Low output will be selected and fed to U10–12. If 2^{1} is 0 (Low) a High output is fed to U10-12.

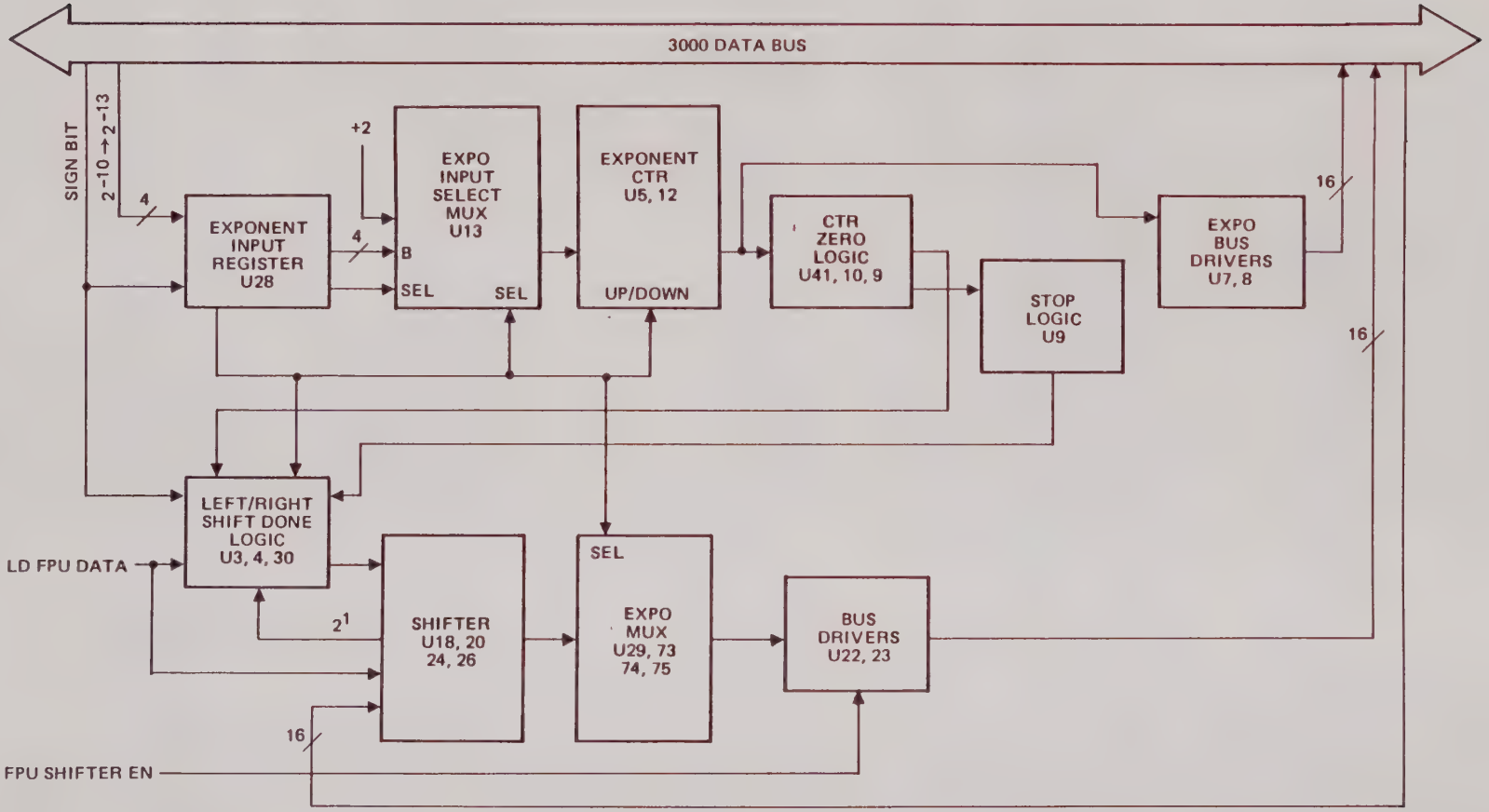


Figure 2-22. FPU Functional Block Diagram (P/O Multiplier A5A10)

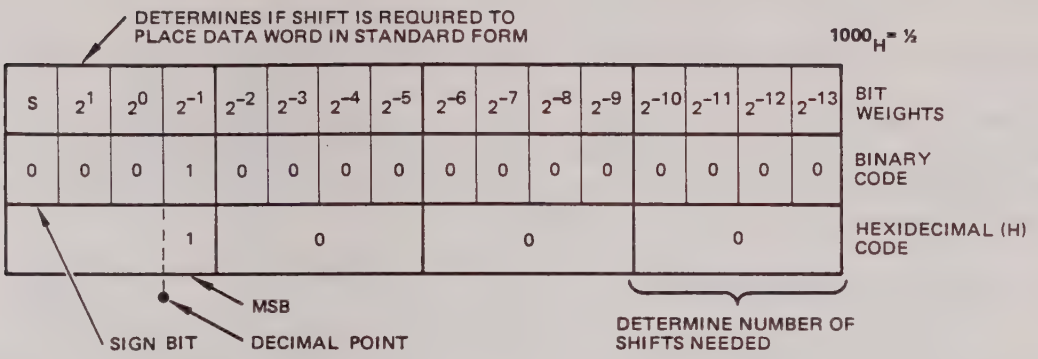

DETERMINES IF SHIFT IS REQUIRED TO PLACE DATA WORD IN STANDARD FORM
$1000_H = ½$
S 2^1 2^0 2^{-1} 2^{-2} 2^{-3} 2^{-4} 2^{-5} 2^{-6} 2^{-7} 2^{-8} 2^{-9} 2^{-10} 2^{-11} 2^{-12} 2^{-13}
BIT WEIGHTS
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0
BINARY CODE
1 0 0 0
HEXIDECIMAL (H) CODE
MSB
SIGN BIT
DECIMAL POINT
DETERMINE NUMBER OF SHIFTS NEEDED

Figure 2-23. FPU Data Bit Organization (Typical Output Form)

Table 2-3. Shifter Function Table

	Inputs						Outputs			
	Mode			Serial		Parallel				
	S1	S0	8 MHz Clock	Left	Right	A B C D	Q_A	Q_B	Q_C	Q_D
LOAD	H	H	↑	X	X	a b c d	a	b	c	d
SHIFT RIGHT	L	H	↑	X	H	X X X X	H	Q_{An}	Q_{Bn}	Q_{Cn}
SHIFT RIGHT	L	H	↑	X	L	X X X X	L	Q_{An}	Q_{Bn}	Q_{Cn}
SHIFT LEFT	H	L	↑	H	X	X X X X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
SHIFT LEFT	H	L	↑	L	X	X X X X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
DO NOTHING	L	L	X	X	X	X X X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{C0}

H = high level (steady state)

X = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

U10 receives its other input from Step Logic Gate U9-6.

With 2 latched at the Exponent Counter (U5, 12) output the Stop Logic puts a low out to U10–11.

The exclusive or gate U2 senses the state of the 2^1 bit. When the input is being normalized both its inputs are qualified if $2^1 = 1$. This makes U10–13 go high to the Shift Left/Right Logic gates U4–2, 4. S_1 then is low and S_0 is high and the Shifter will shift right on the next positive transition of the 8 MHz clock pulse. The EXPO CTR is also decremented by one count.

2.11.6 FPU Operation (Denormalization)

LD FPU # SHIFTS is used to load the four LSBs (2^{-10} through 2^{-13}) plus the sign bit into the Exponent Input Register U28 from the 3000 data bus.

These four low order bits determine the number of shifts to be accomplished to denormalize or return the data to its original binary notation.

A *pull up* on U28–6D (Pin 14) puts an enabling (High) level output on U13 (Exponent Input Selector) to cause it to select the B inputs. In addition the *pull up* enabling level is fed to the Left/Right Shift Logic, the Multiplexer, and the Shift Done Logic (U1).

The EXPO INPUT REGISTER latched output is then loaded into the EXPO CTR by LD FPU DATA.

The sign bit is used to determine the direction of the shift. If the sign bit is a zero (Low level) the binary number is positive; if it is one (1) or (High) the binary data is negative.

A one (1) sign bit will then cause the EXPO CTR to count up through AND GATE U6 as a result of High levels at both inputs (Pins 10 and 9) and driving the UP/DOWN inputs to the EXPO CTR High.

FPU SHIFTER EN to U14–2 (a one shot MV) clears the EXPO Input Register.

2.12 Z80 FUNCTION CONTROL PROCESSOR (A5A8) AND FRONT PANEL INTERFACE (A5A18) ASSEMBLIES

2.12.1 General

The Control Processor (A5A8) and the Front Panel Interface (A5A18) Assemblies combine to (1) control the Z80 Data Bus and the Z80 Address Box, (2) handle interrupt priorities, (3) monitor machine status, and (4) transfer data to and from the MAIL BOX (RAM) to communicate with the 3000 CPE on the Arithmetic Processor Assembly (A5A12). Control signals are generated to coordinate the overall functioning of the Dynamic Analyzer.

2.12.2 Control Processor

The overall block diagram of Figure 2-24 depicts the flow of data, Address, and Control information between the major circuit elements of the Control Processor.

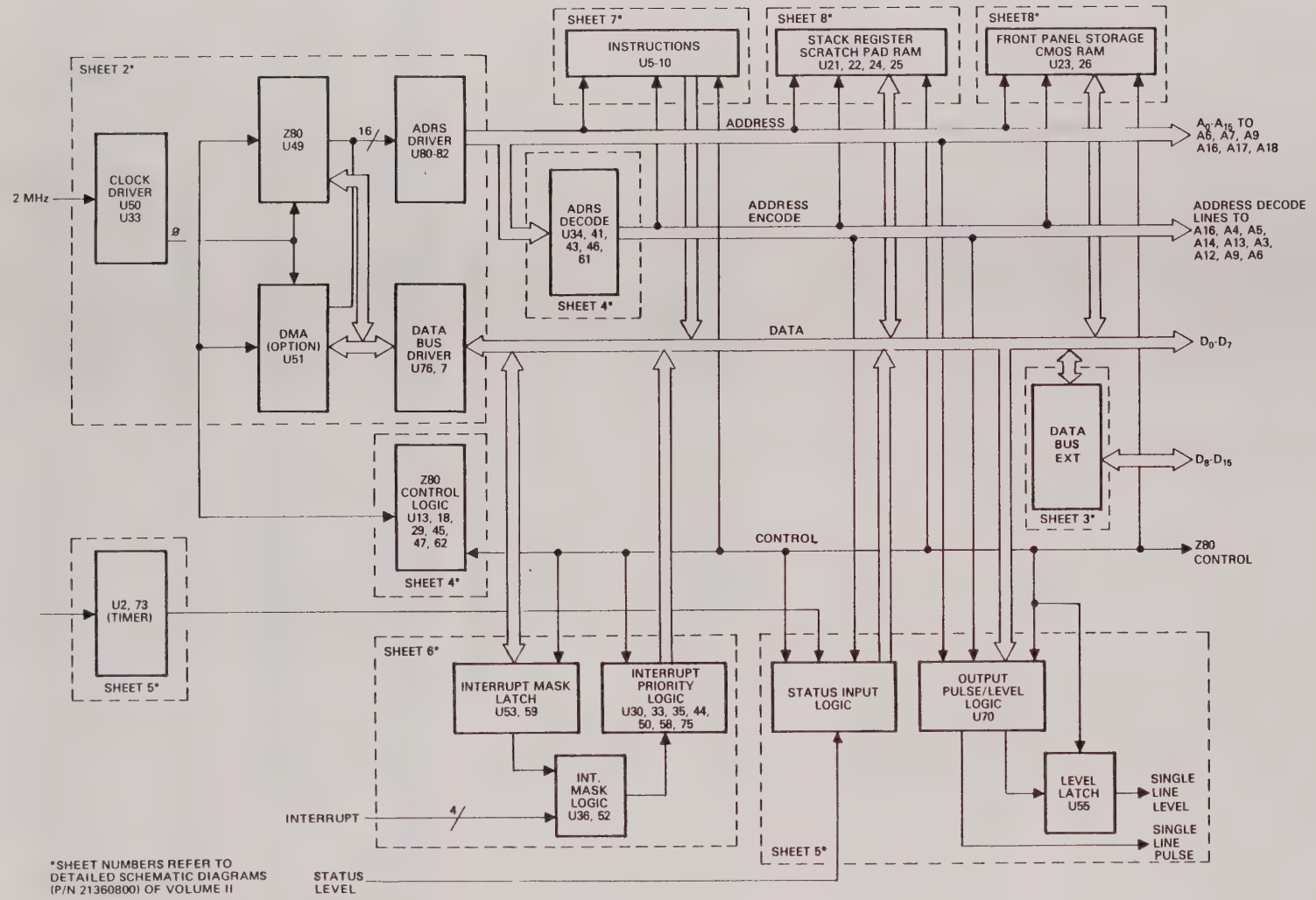


Figure 2-24. Control Processor Overall Block Diagram

2.12.2.1 Z80 Microprocessor (CPU)

The Z80 Microprocessor fetches its instructions from six 4096 × 8 PROMs (U5–10) on the A5A8 board. The Z80 CPU acts on the instructions and transfers information to and from the MAIL BOX to communicate with the Arithmetic processor (A5A12), to set the status and control lines to coordinate the data processing and display functions via the Z80 Control Logic, and monitors the front-panel information via the Z80 DATA BUS. Four 1024 × 4 RSMs on the A8 board are stacked to provide a 1024 × 8 format for the Z80's Stack Register and Scratch Pad.

The Z80 Microprocessor is initialized to Address 0000 by the PWR ON RST (See Schematic 21850000 Sheet 2) to its Reset input. Other internal conditions established by PWR ON RST are as follows:

Reset Interrupt Enable Flip Flop
Clear Program Counter
Clear Index Register
Clear TV Memory Refresh Register
Clear Address Bus and Data Bus to High impedance (Z) states
Deactivate all Control Outputs

2.12.2.2 Direct Memory Access

Hardware accommodations for a Z80-DMA (XU51) were initially designed into the Control Processor PWA but are not currently in use. The Z80-DMA device is therefore not incorporated. All microprocessing functions of the control processor are handled by the Z80-CPU (U49).

2.12.2.3 Z80 Control Logic

The Control Logic on the A8 board consists of the circuitry to decode the Z80 ADDRESS BUS to dedicated control signals. The control signals enable specific memory blocks internal of the Control Processor (A5A8) and in other circuits external to the Control Processor.

The Z80 Control Logic (Schematic Sheet 8) uses five outputs from the Z80 Microprocessor to generate controls used to enable the various internal memory and coordinate operations throughout the instrument.

M_1 (Machine Cycle One) indicates that the current machine cycle is the OP code fetch cycle of executing an instruction. The data in the Instruction PROM is placed on the Z80 data bus and read to the Z80 Microprocessor via Data Bus Transceivers U77 and U76 (Sheet 2).

MREQ (Memory Request) indicates that the Address Bus holds a valid address for a memory read or write operation.

IORQ (Input/Output Request) indicates that the LSB (Least Significant Byte) of the Address Bus holds a valid I/O address for an I/O read or write operation. An IORQ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the Data Bus.

RD (Memory Read) indicates that the Z80 CPU wants to read data from memory or another I/O device. The address I/O device or memory uses this signal to gate the requested data onto the Z80 Data Bus.

WR (Memory Write) indicates that the Z80 CPU Data Bus holds valid data to be stored in the addressed memory or I/O device.

2.12.2.4 Interrupt Priority Logic

The Interrupt Logic on the Control Processor consists of the Interrupt Mask Latch, the Interrupt Priority Logic, and the Internal Mask Logic.

The Z80 CPU sets the Interrupt Mast Latches and Priorities using the control signals (shown on details schematics of Volume II). Masks are set to avoid interrupts during processing periods when data could be lost or the control sequence disrupted. The interrupts signal the CPU that there is a change in status that requires its attention, such as during a transient capture sequence.

Figure 2-25 depicts the daisy chain configuration of the overall instrument interrupt control.

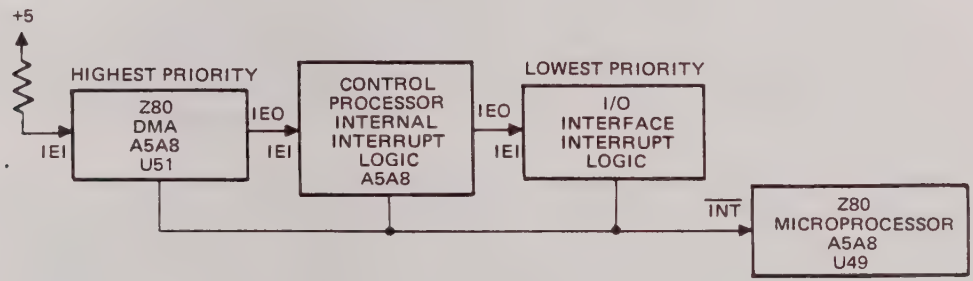


Figure 2-25. Interrupt Control Configuration

At the highest priority is the Z80 DMA which has its Interrupt Enable Input (IEI) tied to TTL high (Active) through pull up resistor A5A5R7. The Z80 DMA Interrupt Enable Output is fed to Interrupt Priority Logic within the A5A8 Control Processor and out as I/O INTERRUPT EN INPUT to the I/O Interface (A5A9) Assembly.

The daisy chain is completed by the I/O INT 1 output from the I/O Interface Assembly to the Z80 CPU Interrupt Request INT input.

An Interrupt Request signal generated by any of the I/O devices within the chain will be honored at the end of the current (in process) instruction cycle in accordance with its priority if the Z80 internal software controlled interrupt enable flip-flop is enabled.

The Control Processor Interrupt Circuitry is part of the simplified block illustrated in Figure 2-26.

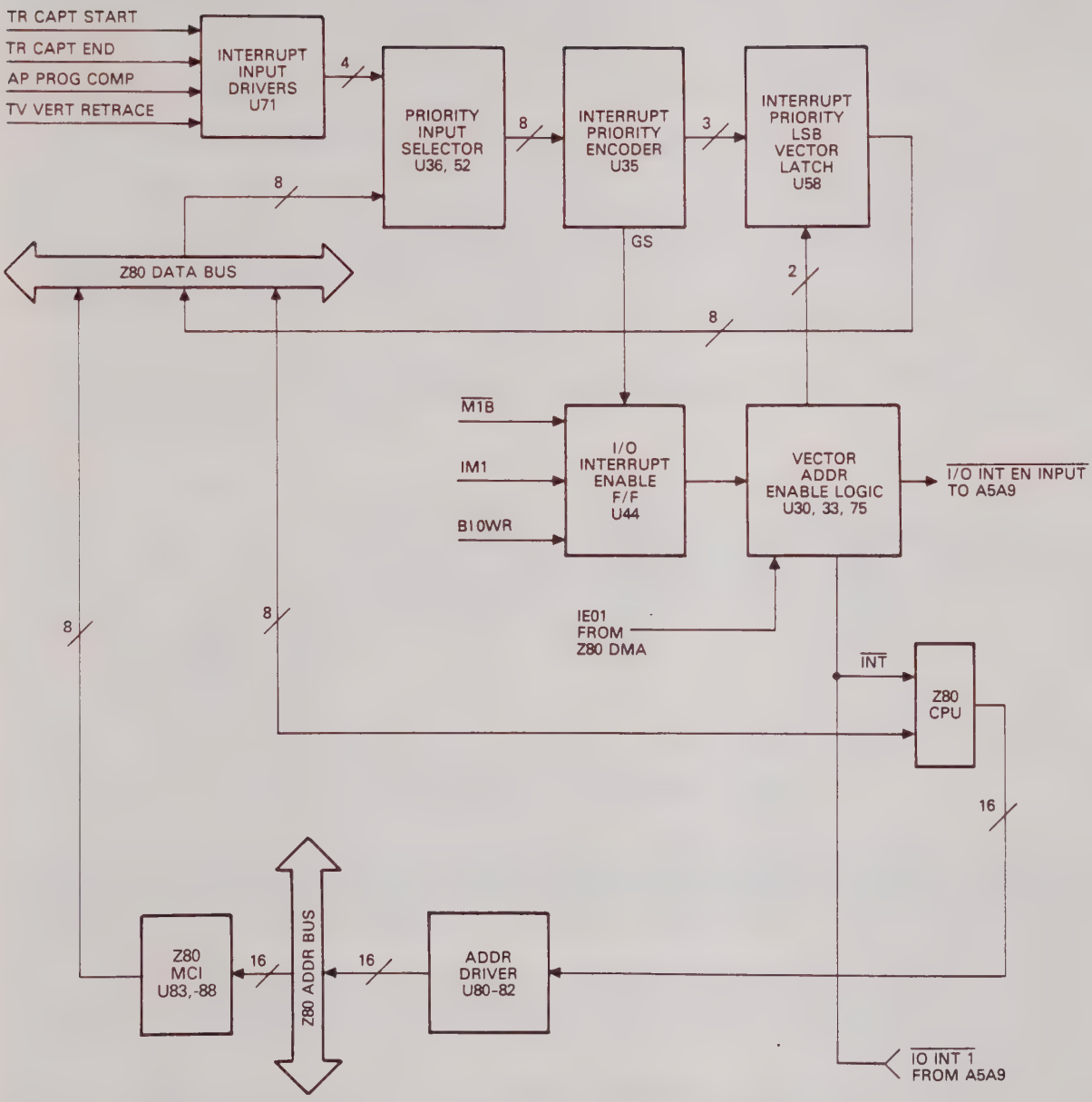


Figure 2-26. Control Processor Simplified Interrupt Circuitry

The Interrupt Mask (U53) will mask the Interrupt inputs placed on the Reset (R) inputs of the Priority Input Selector (U36, 52) when its outputs are equal to zero. The table which follows describes the input/output conditions on the Priority Input Selector.

Priority Input Selector Function Table

Input		Output
$\overline{S}$	$\overline{R}$	Q
L	H	H
H	L	L

H = high level
L = low level

The relative positions of the various interrupt inputs to the Interrupt Priority Encoder (U35) determine their order of interrupt precedence. Input 7 has the highest priority while input 0 has the lowest. The highest priority interrupt handled is TV Vertical Retrace while the lowest priority is TR CAPT START.

The Interrupt Priority Encoder performs the function of ranking the eight interrupt inputs in order of importance and yields an output word (A_0 A_1 A_2) to indicate the highest priority interrupt input present at BIOWR (Buffered Input/Output Write) time.

The GS signal output from U35 goes low to indicate that there is an interrupt needing to be processed. GS is fed to the Interrupt Enable flip-flop (U44-D). When clocked by M1B, U44Q goes high, and, (if it has daisy chain priority) causes the interrupt vector to be placed on the Z80 Data Bus when acknowledged by BINTA. The remaining five bits of the vector are hard-wired zeros. The following chart illustrates Interrupt Priority Encoder outputs which form the VECTOR LSB for the various interrupt inputs received.

Interrupt Priority Encoder Function Table

Inputs									Outputs			
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS
L	H	H	H	H	H	H	H	H	H	H	H	H
L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	X	X	X	X	X	L	H	L	L	H	L
L	X	X	X	X	X	L	H	H	L	H	L	L
L	X	X	X	X	L	H	H	H	L	H	H	L
L	X	X	X	L	H	H	H	H	H	L	L	L
L	X	X	L	H	H	H	H	H	H	L	H	L
L	X	L	H	H	H	H	H	H	H	H	L	L
L	L	H	H	H	H	H	H	H	H	H	H	L

Interrupt Pending logic signals the Z80 microprocessor that an Interrupt Request is being made.

The Z80 microprocessor then reads the 8-bit vector from the Z80 Data Bus as the LSB (Least Significant Byte) of the vectored address in memory of the block of instructions required to service the Interrupt.

The MSB (Most Significant Byte) of the vector address is obtained from the Z80 microprocessor's (I) register. The Z80 CPU (I) register contents plus the LSB Interrupt Vector for the 16-bit address in RAM where the location (in PROM) of the interrupt instruction sequence starting point.

2.12.2.5 Status Logic (General)

Whenever the Z80 microprocessor is not busy with other functions it reads all status inputs and performs the required service routines for each active status input. The active status inputs are processed in the sequence in which they are received or as controlled by Status control logic and Z80 control logic

Some of the Status inputs are maskable (they may be ignored). Maskable and non-maskable status inputs are listed below.

Unmaskable Status	Maskable Status
ENSEMBLE COUNT 0	XLTR OVLD B
SEL EXT SAMPLE FREQ	XLTR OVLD A
80 Hz (TIMER)	AD OVLD B
XLTR	AD OVLD A
IO CARD	AP HALT REQUEST
SEL SD346	PLTR DATA RDY
	AP 1024 PULSE
	OUTPUT OVLD

2.12.2.6 Status Logic Circuit Analysis

The Control Processor Status Monitoring and Control circuitry is illustrated in Figure 2-27. Overall operation of Z80 Control and Status Control Logic functions are also depicted in the block diagram.

The Z80 Address information is decoded to provide control inputs to the Status Control Logic (U59, 60, 75). Masking Latches (U4, U38), as directed by Z80 Control and Status Control Logic, supply masking inputs to Status (S-R) Latches (U19, 37, 29). Z80 Address information is also decoded to read the Status Latches via Bus Drivers (U54, 56, 57) onto the Z80 Data Bus.

Z80 Address Logic is also decoded to read the Z80 Data Bus and latch system control levels (generated by the various status inputs) on the output of Output Level Latch U55. The Bus is also decoded to generate system strobes via Output Pulse Decoder (U70).

Detailed schematics of the status monitoring hardware is contained in Volume II (drawing 21850000 sheet 5). Use of the detailed schematics is encouraged when additional information is required.

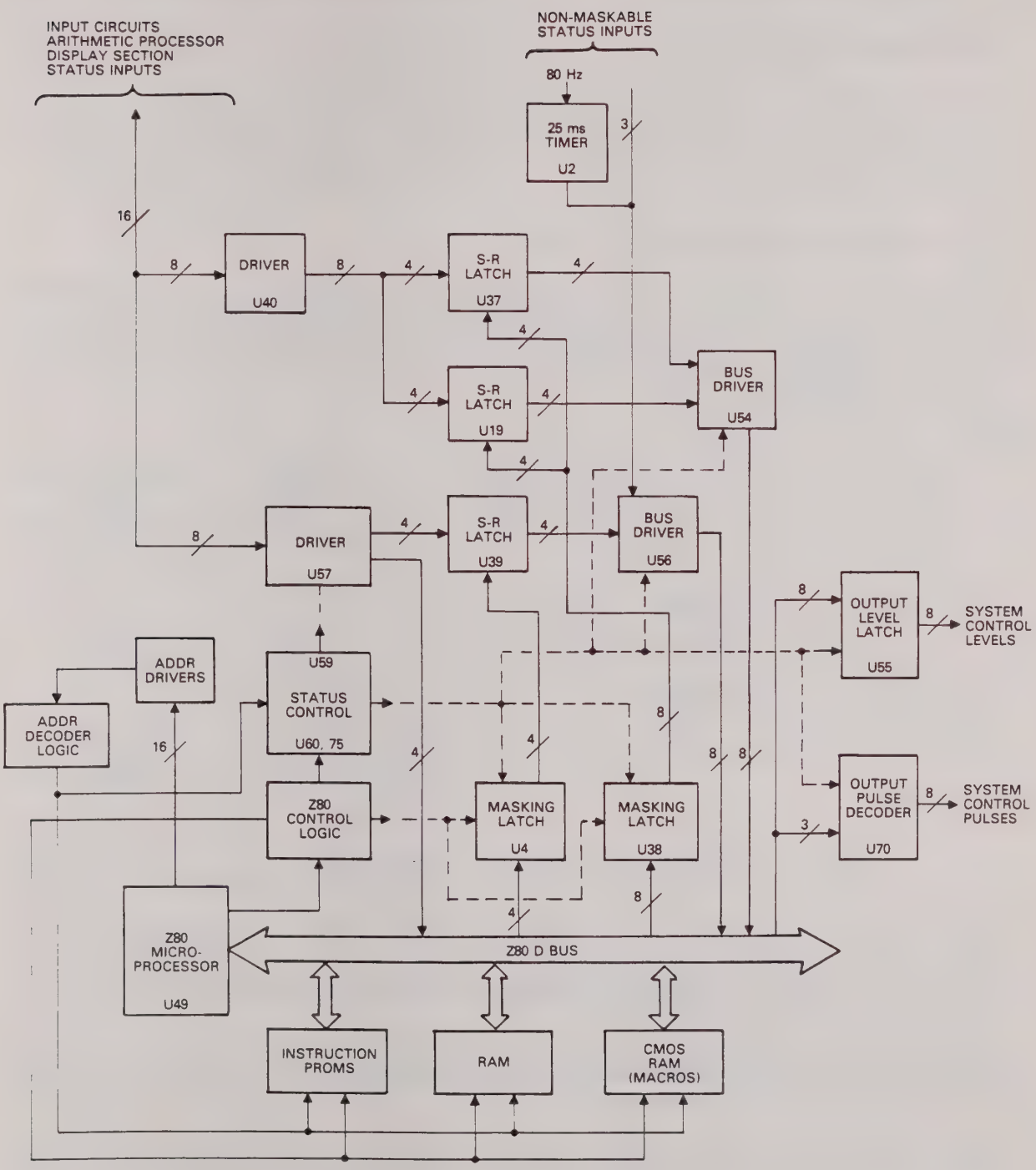


Figure 2-27. Control Processor Status Monitoring and Control Detailed Block Diagram

2.13 FRONT PANEL INTERFACE

2.13.1 General Description

The primary functions of the Front Panel Interface Assembly (A5A18) are (1) the generation of system macro instructions based on front panel touch control (or remote control) inputs for the Control Processor and (2) coordinate the exchange of data between the Arithmetic Processor (A5A12) 3000 CPE and the Z80 microprocessor.

2.13.2 Front Panel Interface Operating Concept

Front panel inputs are made by the operator using the touch controls of the keyboard matrix. When a touch control is depressed a signal is transferred from the Row Decoder through the front panel matrix via the depressed switch to the column encoder and is placed on the Z80 data bus to the Switch Data RAM (as depicted in Figure 2-28 below).

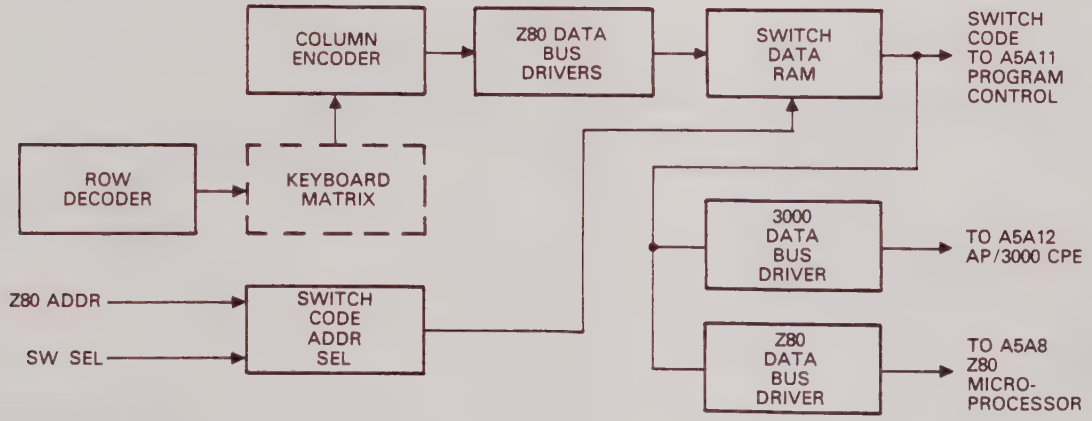


Figure 2-28. Front Panel Control/Interface Simplified Block Diagram

The Switch Data RAM stores the switch code data which is read by the 3000 CPE on A5A12 (Arithmetic Processor), the Z80 microprocessor on the Control Processor (A5A8), and is feed to the Microprogram Control Assembly (A5A11) as a Jump Offset for the address generator which accesses instruction words to the control the functions of the 3000 CPE.

The keyboard entry monitoring processor is accomplished by the Z80 microprocessor when it is not busy with coordination of other system functions.

2.13.3 Detailed Circuit Analysis (Keyboard Entry)

The following analysis of Front Panel Control (A2) and Front Panel Interface (A5A18) hardware is developed around the detailed block diagram (Figure 2-29) and schematics as follows:

Assembly	Drawing No.	Sheets
Front Panel Control (Matrix)	21210100	6, 7
Front Panel Interface	21149700	2, 3

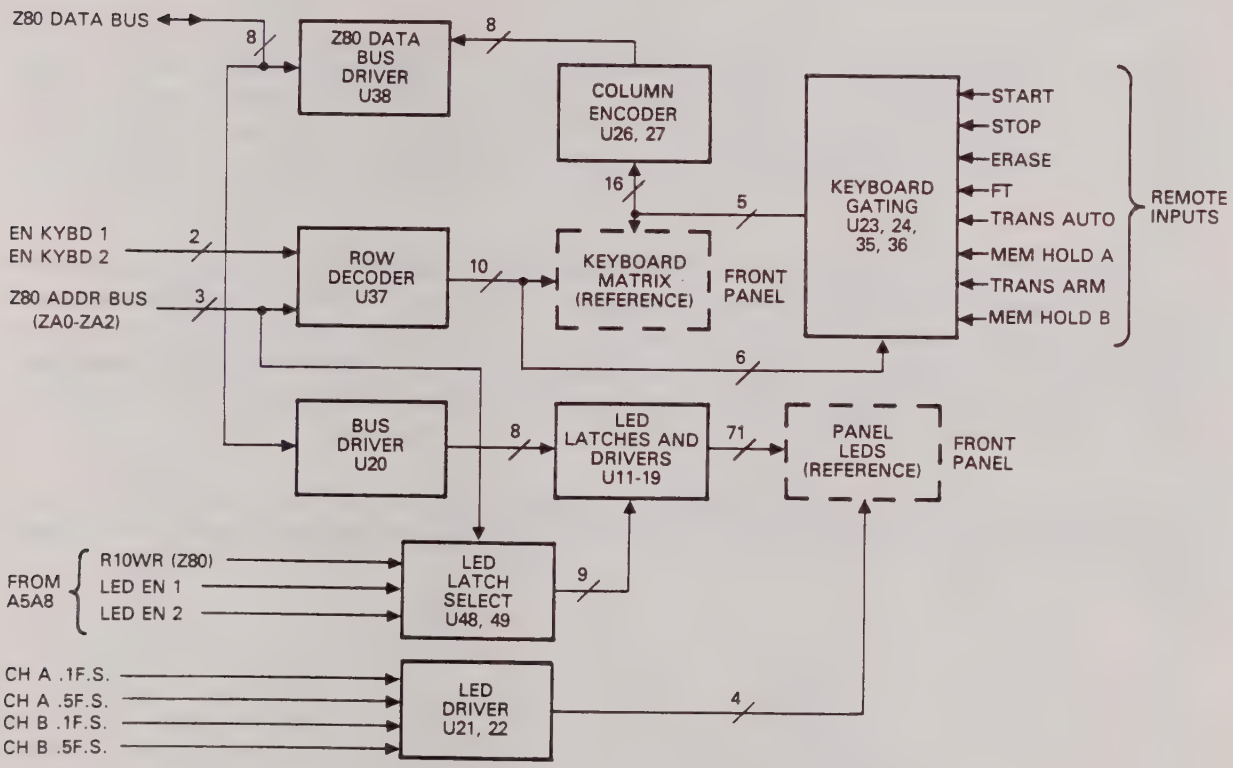


Figure 2-29. Front Panel Control/Interface Detailed Block Diagram (Keyboard Entry)

A type SN 74154 4 to 16 line decoder is employed as the Row Decoder (A5A18U37). It supplies ten active low (ground) outputs to the front panel matrix as selected and decoded from Z80 Address Bus (bits A0 - A2) and EN KYBD 1 inputs.

When a switch is selected (depressed), the low or ground is transferred to the Column Encoder (A5A18 U26 and U27), which develops Octal Output Code of the row and column of the depressed switch.

The Binary Octal output of the Column Encoder is placed on the Z80 Data Bus via drivers U38 to the Switch Data RAM (A518U56) and to driver (A5A18U20), to drive the appropriate LED.

The same three Z80 Address bits used by the Row Decoder (U37) are decoded by the LED Latch Selector (A5A18U48 and U49) to select the corresponding LED Latch/Driver and provide a (low) ground to the appropriate front panel LED.

Overflow inputs from Signal Conditioners A and B (A5A1 and A5A2) are fed to drivers (U21, sheet 1 of drawing 21149700) to appropriate Front Panel LEDs.

2.13.4 Front Panel Interface Assembly (Arithmetic Processor/Z80 Microprocessor Data Exchange)

The following detailed analysis refers to Figure 2-30 and Front Panel Interface (A5A18) drawing number 21149700 (sheet 2).

The heart of the Data Exchange circuitry is the Mailbox RAM (A5A18U40-U43), a 256 word by 16-bit RAM that is addressed by either the 3000 CPE or the Z80 microprocessor. The Mailbox is written to or read from by either the Z80 microprocessor or the 3000 CPE. Switch code data is accessed by Microprogram Control (A5A11), 3000 CPE, or the Z80 as determined by Microprogram Control (A5A11).

The Mailbox RAM stores the macro strings (a sequence of instructions used to execute all required subroutines based on Front Panel Inputs) used to process input data. The Mailbox receives its inputs from the Z80 as a result of the Z80 acting on instructions it fetches from Control Processor Instruction PROMs (A5A8U83-U88). The Mailbox information is then accessed by the 3000 CPE via 3000 Data Bus Drivers (A5A18U53 and U54). 3000 CPE data stored in the Mailbox is accessed by Z80 Bus Drivers (A5A18U52 and U55).

The Clock Gating Circuit (A5A18U21, 34) located on the A18 board latches Z80 data (Display Mode, Cursor Mode and Trace data) into the Mode Latch (A5A18U50). This information is fed to Cursor Control Assembly (A5A14).

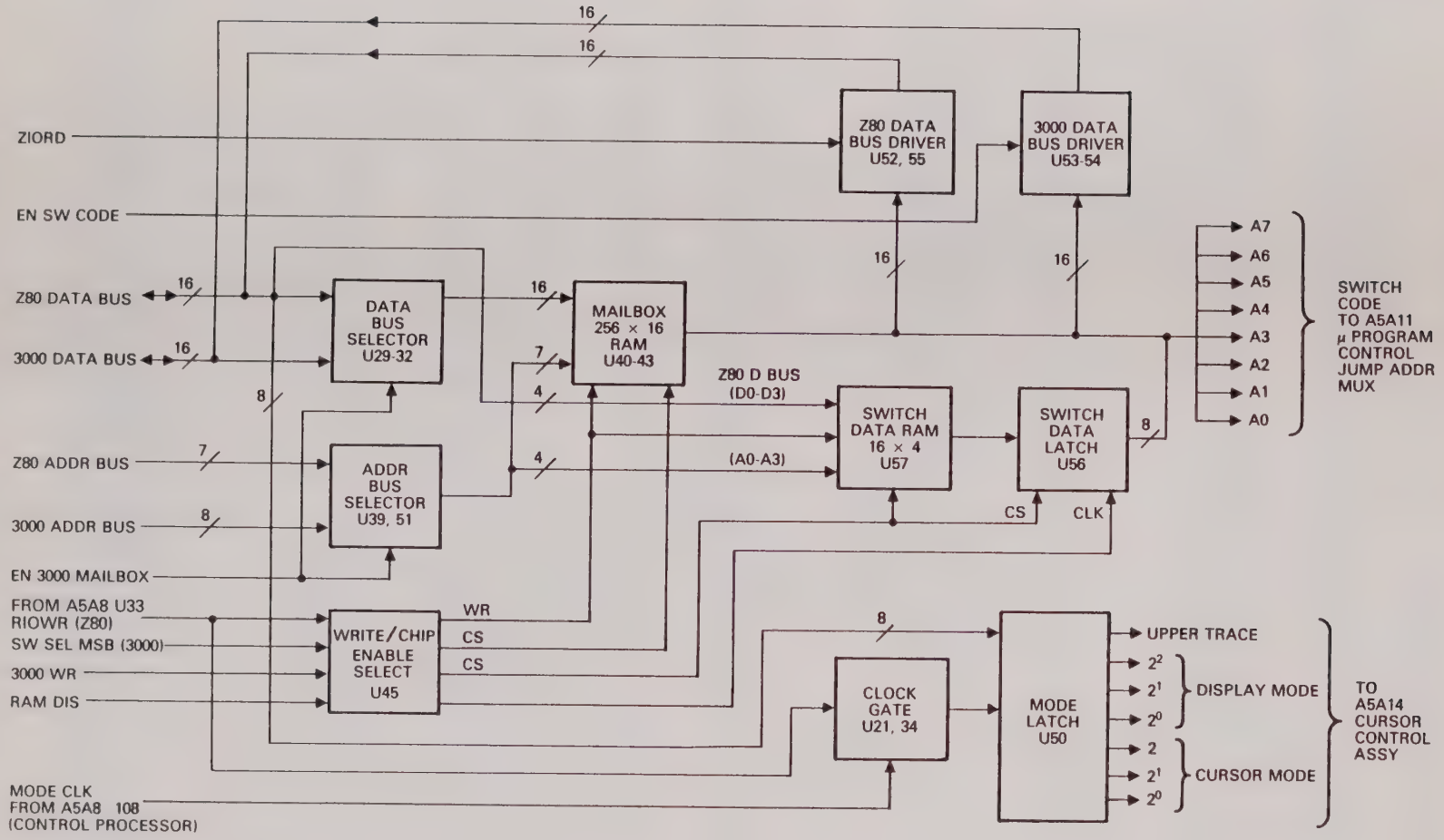


Figure 2-30. Front Panel Interface Assembly-Control Processor/Arithmetic Processor Data Exchange Circuitry (Simplified)

2.14 VIDEO INTERFACE ASSEMBLY

The Video Interface Assembly (A5A16) consists of the circuitry which processes vertical data for display, generates crt graphics and generates the crt grid. All of the above functions are accomplished under control of TV Timing Logic.

Figure 2-31 is an overall block diagram of the Video Interface Assembly. the major circuit elements of Video Interface Assembly consist of TV Timing Logic, TV Memory; the Character Generator, the Grid Generator, and the TV Video Output.

2.14.1 TV Timing Logic

The following paragraphs refer to Figure 2-32 (TV Timing Logic Simplified Block Diagram) and Video Interface Assembly Schematic (drawing number 21860100 sheet 2).

Fundamental timing is generated by Y1 (a 43.343 MHz oscillator) which feeds Binary Counter U39. The divide-by-5 output (known as F409) is 8.469 MHz provides fundamental display timing for frequency domain (Spectrum) modes. The divide-by-two output from Counter U39 is counted down by U20 to provide F512 (the 10.586 MHz clock frequency) used in time domain display operations.

2.14.2 Display Timing

System Display Timing is controlled by Timing PROMs TXA and TYA (the x-axis and y-axis memory devices A5A16U1 and U12 respectively). These two PROMs control all functions required to generate the video display.

TXA is driven by TXA Address Counter U2, U20 which is clocked by F409. The outputs of TXA are latched by the TXA Address Counter LSB to U3.

The 2^0 bit (LSB) from X-Axis Timing PROM (U1) is fed through Latch U3 to the Y-Axis Timing Counter (TYA Address Counter U11). The TYA Address Counter generates Y-Axis address bits ($Y_0 - Y_7$) for use coordinating Y-Axis blanking, retrace and synchronization through Y-Axis Timing PROM (U12) and Latch U29. The TYA Address Counter also feeds Y-Axis address bits to the Memory Select and Grid Generation sections of the Video Interface Assembly.

The 2^1 bit (X CTR RESET) from the TXA PROM is used to clear the X-Axis Address Counter (U54) via X-Axis Counter Toggle U26. The X-Axis Counter is driven by X CTR CLK from Clock Selector A5A16U88 (see schematic 21056300 sheet 2). Its eight output bits are fed to Grid Generation and Memory Select circuitry.

2.14.3 TV Memory

The TV Memory section of the Video Interface Assembly is comprised of two 10K memory sections (Memory A and Memory B), a Memory Address Counter (A5A16U55, 57, 38) Clock Selector (U88), TV Memory Chip select and write enable logic. A simplified block diagram of the TV Memory appears in Figure 2-33.

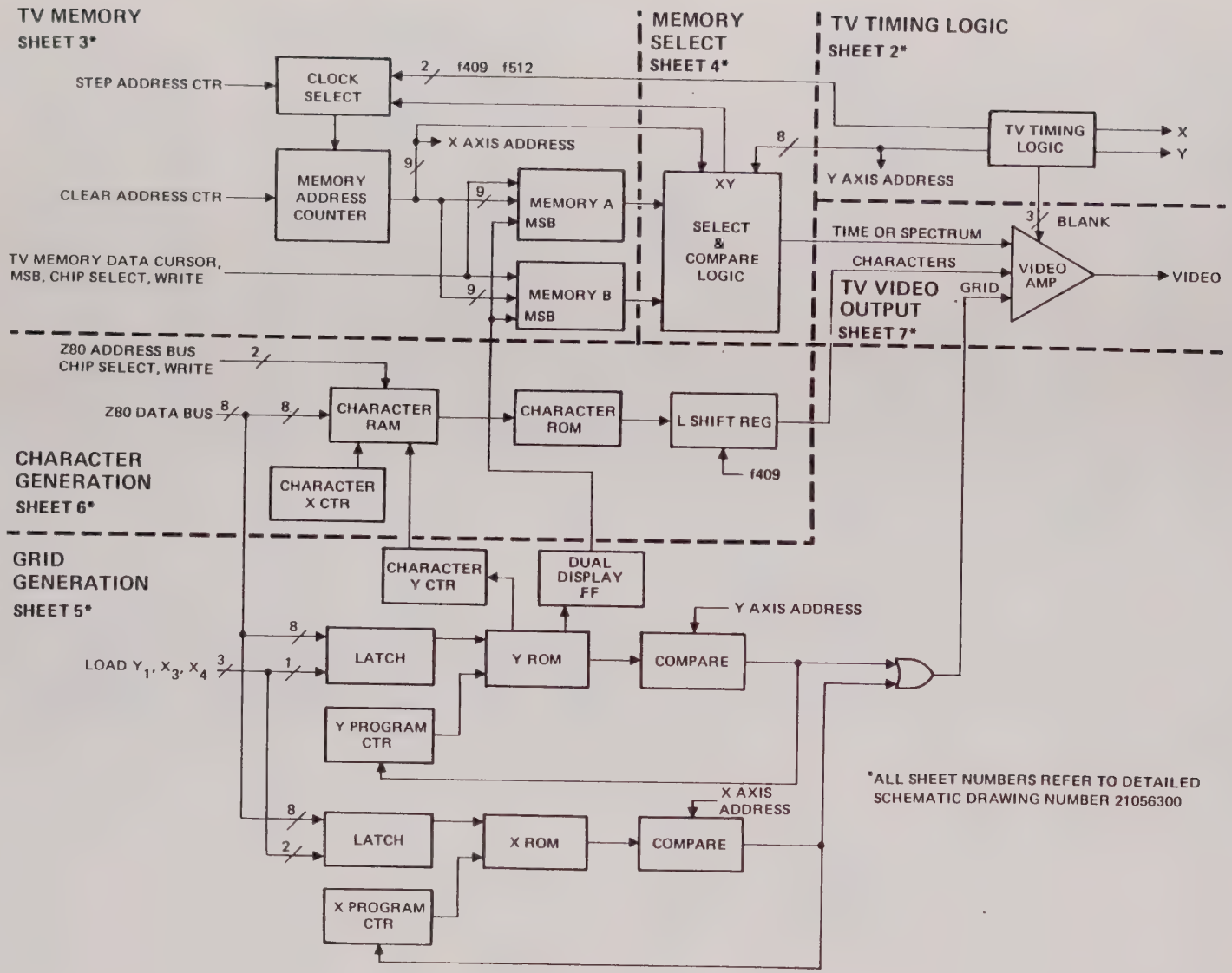


Figure 2-31. Video Interface (A5A16) Overall Block Diagram

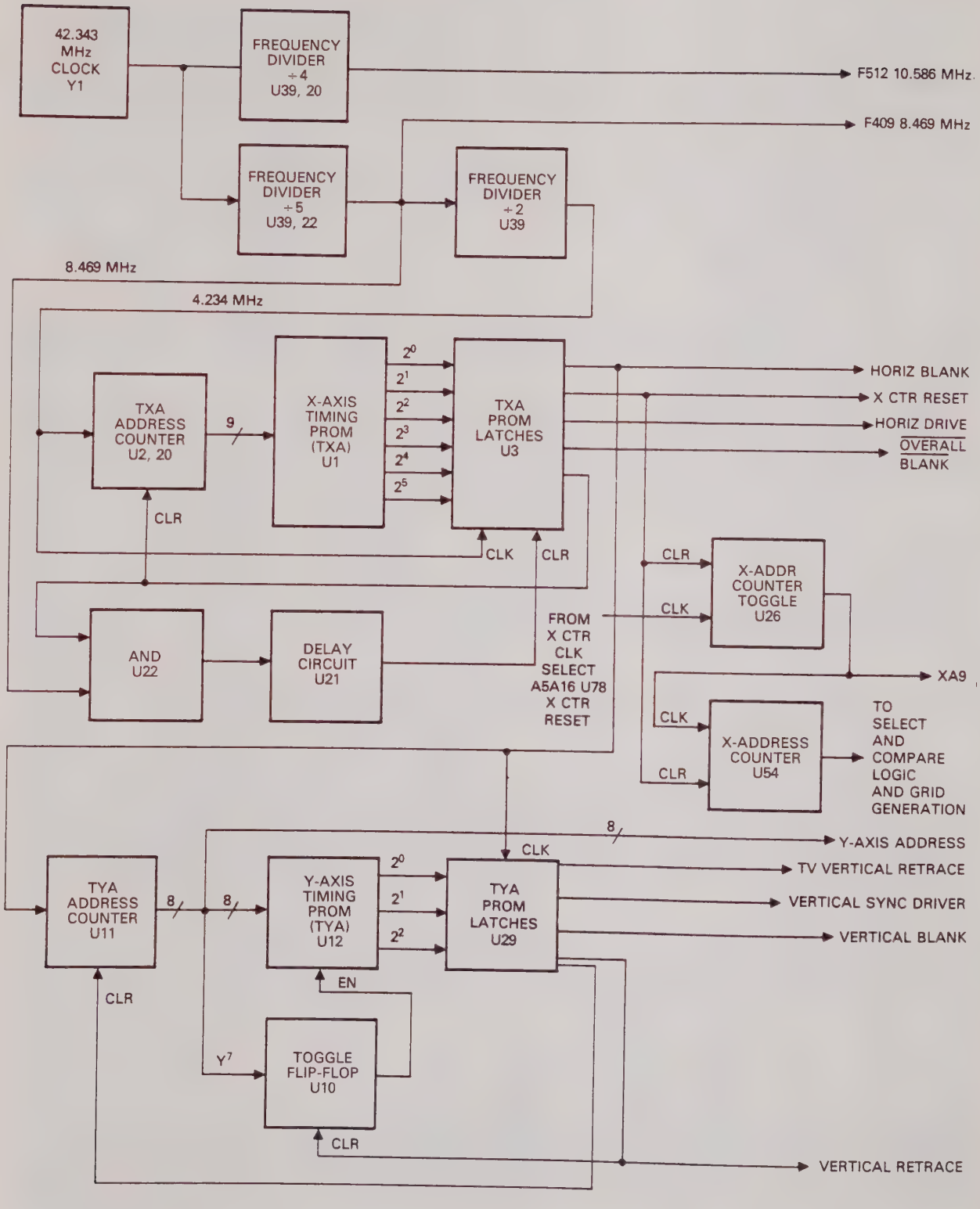


Figure 2-32. TV Timing Logic Simplified Block Diagram

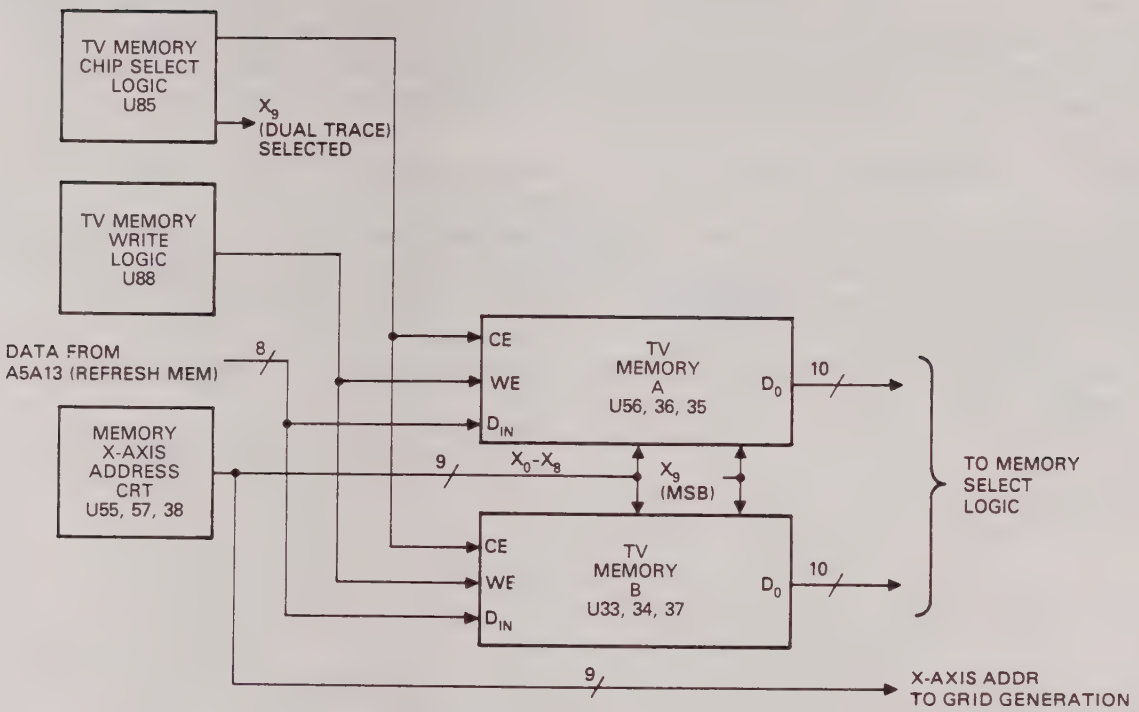


Figure 2-33. TV Memory (Simplified)

The TV Memory of the Video Interface Assembly is loaded with the Y-Axis data written from the Processor Memory (A5A13) Assembly Refresh Memory.

The TV Memory is read by X-Axis Address Ctr bits X_0 through X_8 with the X_9 bit from Chip Selector U56 accessing lower trace data when the Analyzer is operated in the dual trace mode. This is accomplished through Dual Display Flip-Flop (U19).

2.14.4 Memory Select Circuitry

The Memory Select Circuitry located on the Video Interface Assembly has several functions as outlined below:

To control the reading of TV memory data, cursor dot and cursor line to the TV Video Output circuits via the X-Axis Address Counter (A5A16U55, 57, 38).

Select appropriate timing for frequency or time domain dual display operations.

Determine where the cursor is in relation to displayed data when X2 or X4 expanded sweeps are used.

The Memory Select circuitry accepts four primary inputs; (1) TV Memory A data, (2) TV Memory B data, (3) X-Axis Address bits, and (4) Y-Axis Address bits. The Memory Select circuitry provides two primary outputs including (1) frequency or time domain video from the TV Memory, and (2) the X-Y Clock signal (ADV X CLK) to the TV Memory X-Axis Address Counter.

Figure 2-34 is a detailed block diagram of the Memory Select circuitry on the Video Interface Assembly.

The Memory Select circuits employs Band A and B Detector PROMs (U60, U83) to detect when the TV member data A or B bits addressed are with ± 50 cells of the cursor location on times four (X4) expansion (± 100 cells on times two (X2) expansion) via U66 and U66 for frequency domain displays.

The Band Detector PROMs then produce *In Band*, *Below Center*, and/or *At Center* outputs to produce the displayed cursors.

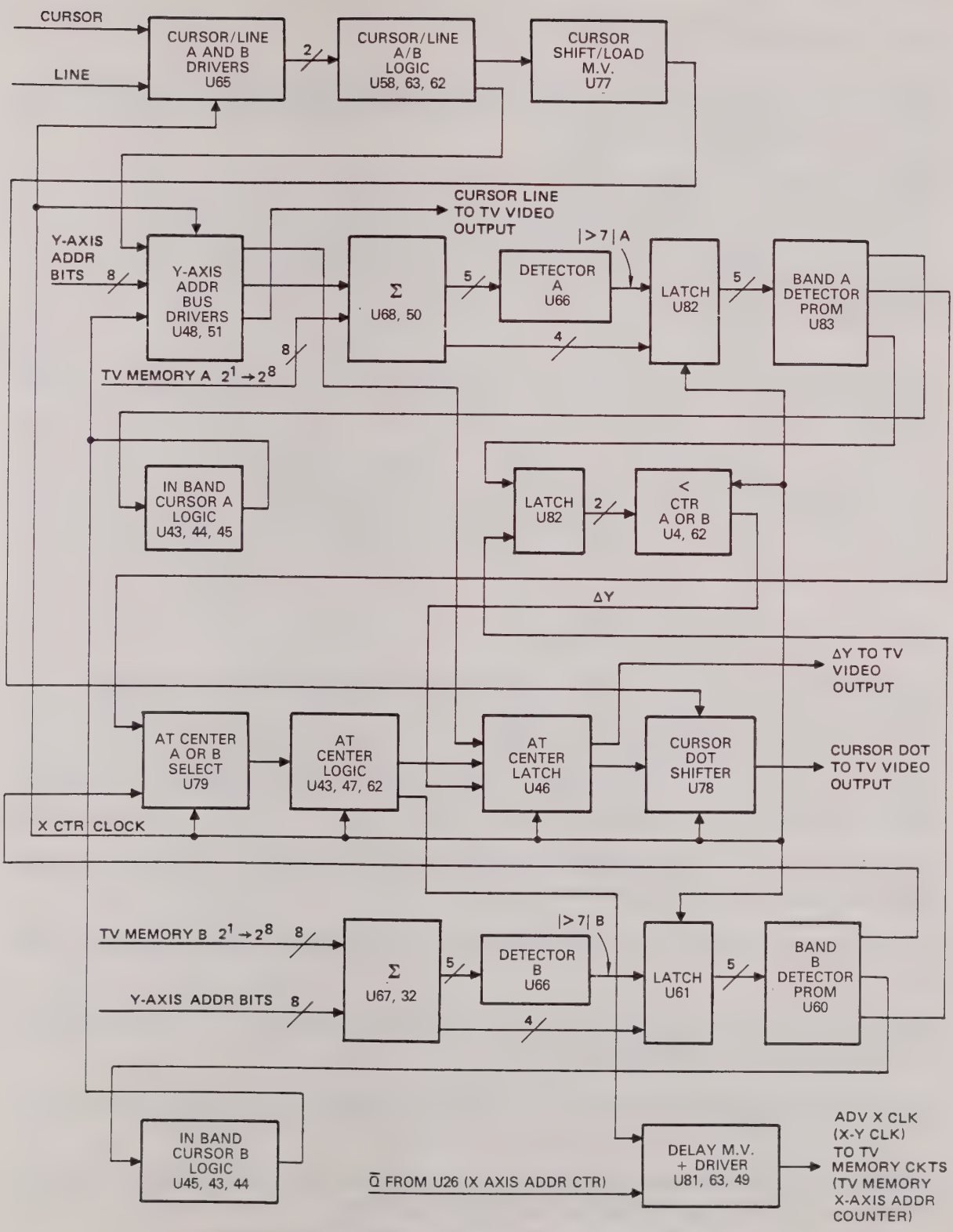

CURSOR
LINE
CURSOR/LINE A AND B DRIVERS U65
2
CURSOR/LINE A/B LOGIC U58, 63, 62
CURSOR SHIFT/LOAD M.V. U77
CURSOR LINE TO TV VIDEO OUTPUT
Y-AXIS ADDR BITS 8
Y-AXIS ADDR BUS DRIVERS U48, 51
Σ U68, 50
5
DETECTOR A U66
|>7| A
LATCH U82
5
BAND A DETECTOR PROM U83
4
8
TV MEMORY A 2^1 → 2^8
IN BAND CURSOR A LOGIC U43, 44, 45
LATCH U82
2
< CTR A OR B U4, 62
ΔY
ΔY TO TV VIDEO OUTPUT
AT CENTER A OR B SELECT U79
AT CENTER LOGIC U43, 47, 62
AT CENTER LATCH U46
CURSOR DOT SHIFTER U78
CURSOR DOT TO TV VIDEO OUTPUT
X CTR CLOCK
TV MEMORY B 2^1 → 2^8 8
Y-AXIS ADDR BITS 8
Σ U67, 32
5
DETECTOR B U66
|>7| B
LATCH U61
5
BAND B DETECTOR PROM U60
4
IN BAND CURSOR B LOGIC U45, 43, 44
Q̄ FROM U26 (X AXIS ADDR CTR)
DELAY M.V. + DRIVER U81, 63, 49
ADV X CLK (X-Y CLK) TO TV MEMORY CKTS (TV MEMORY X-AXIS ADDR COUNTER)

Figure 2-34. Memory Select Circuits Detailed Block Diagram

2.14.5 Grid and Character Generator Circuits

2.14.5.1 Grid Generator Circuit Operation

The Grid Generator Circuitry overall block is shown in Figure 2-31. The detailed circuit analysis which follows will refer to the overall block diagram, the detailed block diagram (Figure 2-35), and the detailed schematic (drawing number 21860100 sheet 5).

From the Control Processor (A5A8) Z80 Address Logic control signals (LD Y GRID, LD X GRID 1, and LD X GRID 2) are received to latch scaling Instruction Bits placed on the Z80 Data Bus into the Y Program, X_3 Program, and X_4 Program Starting Latches. These latched scaling inputs address the appropriate blocks in X-Line, Y-Instruction ROMs (U91, U17, and U16 respectively). The X and Y Program Counters (U28 and U92) provide low order address bits to the ROM and are incremented by Comparator (U93, 73) outputs.

The Y Instruction ROM (U16) provides control and gating levels to the Y Character RAM Address Counter (U92), the Border Blanking Flip-Flop, the dual display flip-flop and to the Grid Bit Logic (U43, U27, U80).

The X and Y Line ROMs (U91, U17) feed comparators (U93, U73 or U31, U14 respectively). X and Y-Axis Address inputs from the TV Timing logic and TV Memory circuits are compared with Line ROM outputs to grid bits when the X-Axis or Y-Axis Address inputs equal X or Y Line ROM outputs. The X and Y Program Counters are then incremented to the Address in X or Y Line ROM of the next grid components.

2.14.5.2 Character Generator Circuit Operation

The Character Generator circuits on the Video Interface Assembly generate all alphanumerical data displayed on the Raster Scan crt. Character Generation (refer to Figure 2-36 and schematic drawing number 21860100 sheet 6) is accomplished by addressing the Character Generator (U64) directly via the Z80 Data Bus through gated Bus Drivers (U70), or indirectly by either Z80 Address Bus or Character RAM X Address Counter bits from U75 and Character Y Counter bits (A0–A3) from the Grid Generator circuitry as selected by U69, 94, 74.

The Character RAM (U72, 71) is loaded with the 6-bit binary words required to access the display alphanumerics when directed by Z80 MEM WRITE.

The Character RAM is divided into two blocks which are addressed by CHAR MEM CS to the chip select inputs.

The Character RAM is read by placing the selected 6-bit Y Address and the 4-bit X Address from the X and Y Address Selectors to the address inputs.

The 6-bit Character RAM output is then fed to the Character Generator (U64), latched by the output of U5, and decoded internally to select the memory location of the desired ASCII character.

The desired character is then read out serially (in bit sequence) through a shifter when clocked by DOT CLK and the Character Generator has the low LD EN signal input.

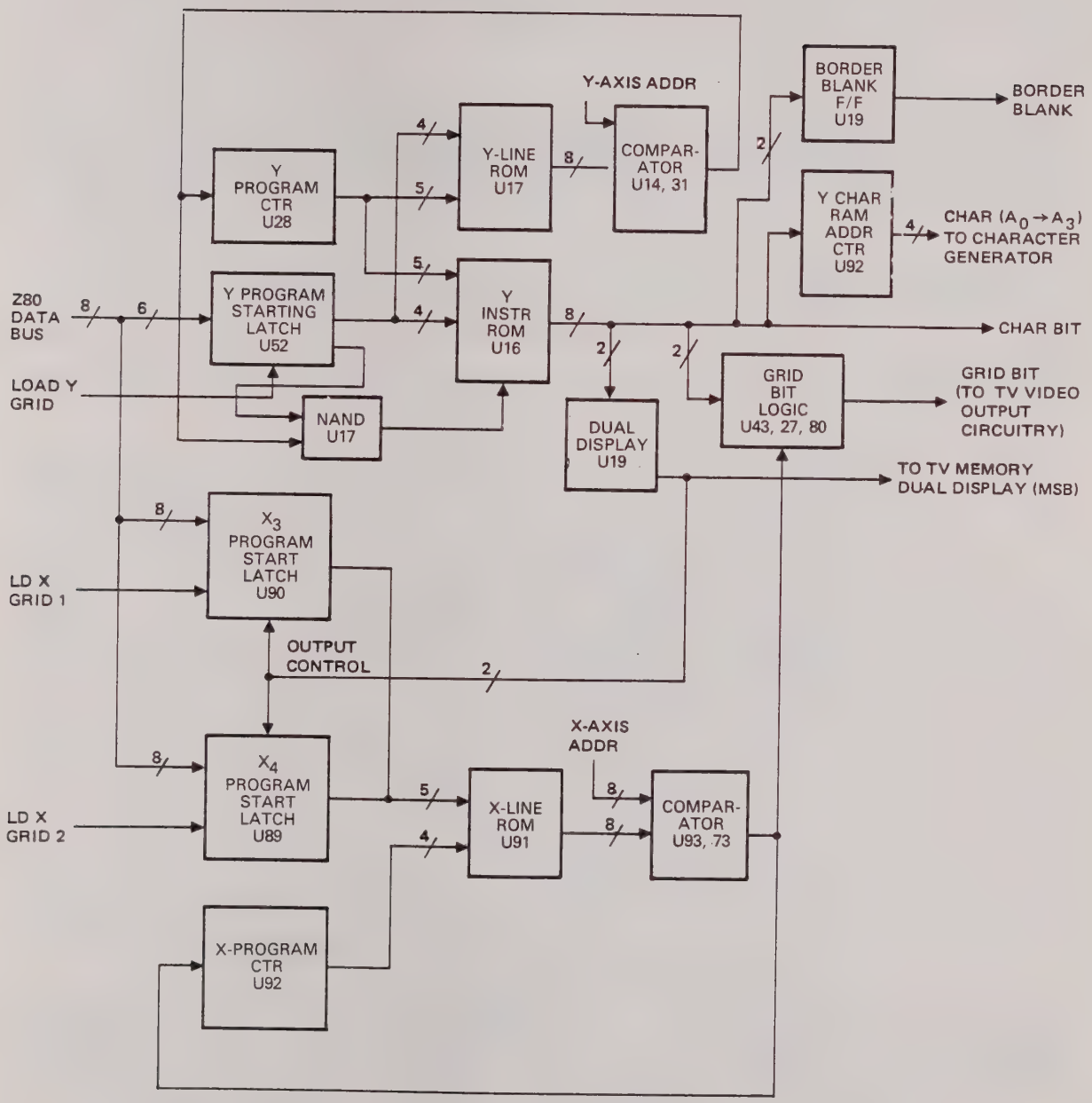


Figure 2-35. Grid Generator Detailed Block Diagram

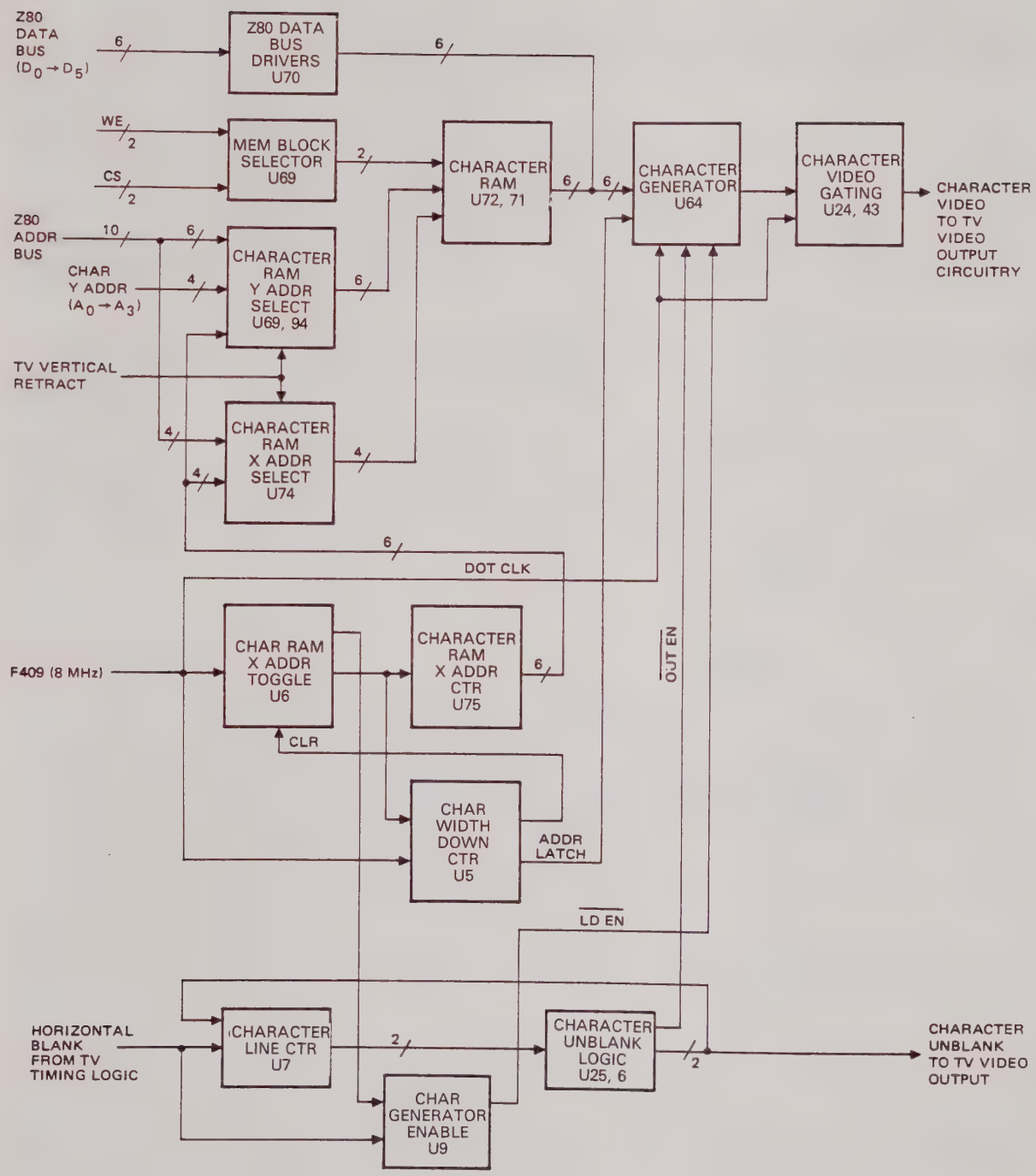


Figure 2-36. Character Generator Detailed Block Diagram

The 8 MHz F409 input to the Character Generator (U64) and the Divide by 8 Counter (U5) provide fundamental timing for character generation. U5 is loaded to a count of seven (0111) and counted down to zero by F409 with its 2^2 bit fed to the Character Generator as the latching signal that latches address bits from Character RAM to the internal address decoders on U64. U5 allows for seven (7) DOT CLK input periods required to generate the output character.

2.14.6 TV Video Output Circuitry

The TV Video Output circuitry (Figure 2-37) accepts the time and spectral data, cursor, grid bits, blanking and sync inputs (as supplied from the other Video Interface circuitry) and mixes these inputs to provide TV video to the crt. A composite video signal is fed to an external video monitor along with horizontal/vertical sync signals for remote controlled video monitors.

The Front-Panel "Grid" intensity control provides for the exclusive control of the grid intensity via Q1 to the Broadband Video Driver (U40). The "Contrast" potentiometer on the front panel provides a range of control over the entire video display through Switch Driver Q2.

Delay Multivibrator (U76) provides horizontal sync outputs on the composite video signal through Video Driver Q4.

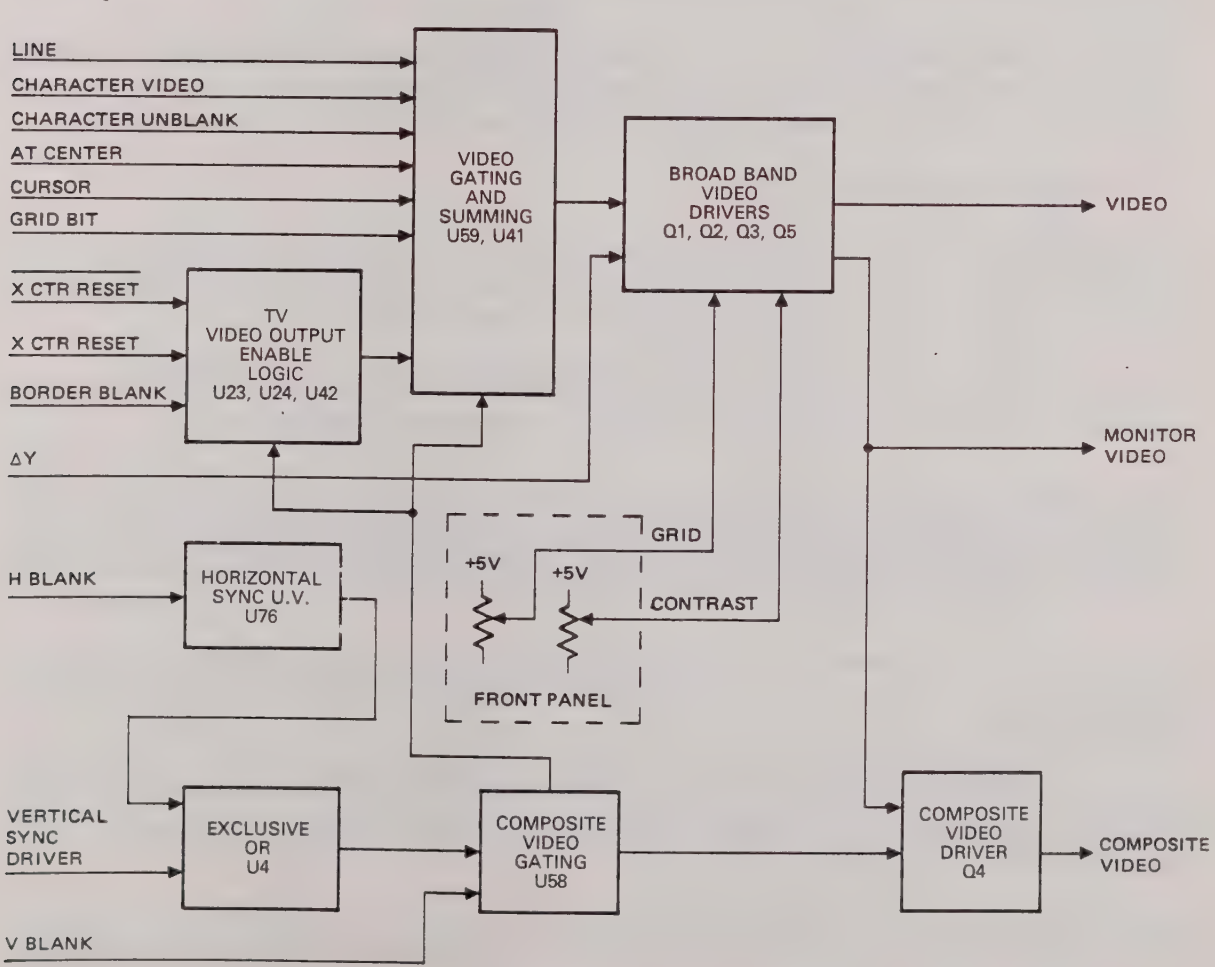


Figure 2-37. TV Video Output Circuitry

2.15 CURSOR CONTROL ASSEMBLY

2.15.1 General Functional Description

The Cursor Control (A5A14) assembly functions primarily to control the access to Refresh Memory located on the Processor Memory (A5A13) Assembly. Cursor Control hardware continuously reads the crt display data written to Refresh Memory by the Arithmetic (3000) Processor and generates control signals for an external X-Y scope. The Cursor Control Assembly transfers Refresh Memory data to the Video Interface (TV) Assembly (A5A16) during vertical retrace time. Display Control logic is employed to provide arbitration for the three (3) users of the Refresh Memory (A5A16 — Video Interface circuitry, A5A12 — Arithmetic Processor, and A5A14 — Cursor Control).

Logic circuitry contained on the Cursor Control Assembly is also used to position the cursor and to generate harmonic dots.

There are three major groups of hardware associated with Cursor Control: the Display Control Processor, cursor position circuits, and Transfer Control Logic.

The functional description of each of the aforementioned hardware groups is covered in the paragraphs which follow. Detailed wiring diagrams of the Cursor Control (A5A14) circuitry which are referred to throughout this section are contained in Volume II of this manual as drawing number 21084200.

2.15.2 Display Control Processor

The Display Control Processor circuitry is composed primarily of a multiplexer (Test Selector U48–50), an Address Generator (U3, U16), a 4K (512 × 8) Read Only Memory (U14, 15), Output Pulse Decoders (U20, 21) and Output Level Latches (U2), which are illustrated in Figure 2-38.

The Display Control Processor generates the instruction sequences required to accomplish all functions of the Cursor Control Assembly (outlined in the general functional description above).

The Test Selector (U48–50) monitors numerous internal and external Cursor Control functions as dictated by the Control PROMs (U14 and 15) and branches to appropriate instruction sequences based on test results. The Test Selector produces a branch control signal which loads the address of the first instruction of the branch subroutine into the Address Generator (U3 and 16).

Strobe Decoder (U20, 21) outputs are fed to Test Selector Input Logic (shown in Figure 2-39) and determine what branches are made by the PROM Controlled Sequencer/Address Generator based on display parameters entered.

Control PROM (CURS 1–U14) provides coded bits to Chip Selector (U1) which determine which machine state is tested and also provides coded bits to the Output Strobes Decoder (U20, 21) for generating required display controls.

Control PROM (CURS 2–U15) supply X-Counter Preset bits to the X-Y Scope Display Address Counter and Control levels via Level Latch (U2). Control PROM Bit Configuration is depicted in Figure 2-40.

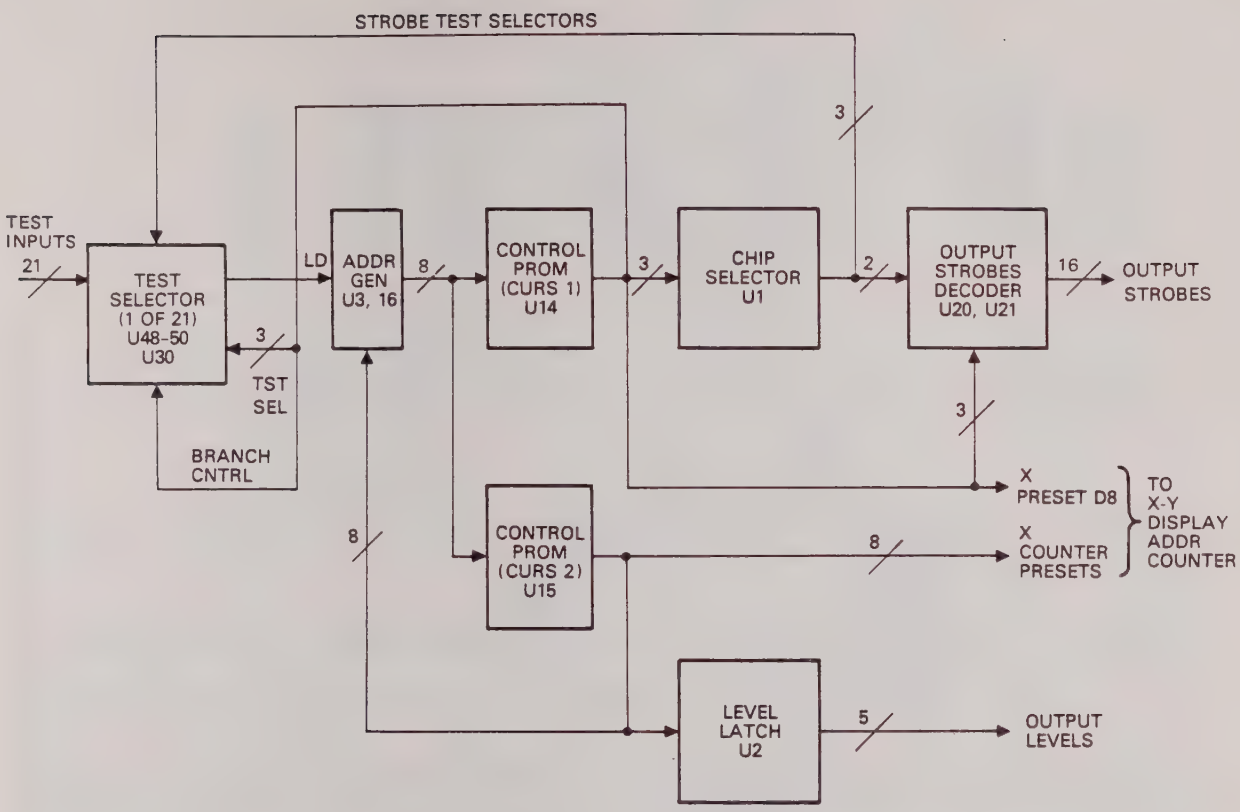


Figure 2-38. Display Control Processor (P/O A5A14 Cursor Control Assembly)

2.15.2.1 Display Control Program

The Display Control Program (typified in Figure 2-41) for the Cursor Control Assembly is stored in CURS 1 and 2, and is sequenced by the 8-bit Address Generator until the branch control to the Test Selector produces low at TP5. When this occurs, Counter presets are loaded into U3 and 16 (the address of the branch subroutine.

The Display Control Program operates typically as follows:

If there is a 3000 request, it allows the 3000 CPE to use the Refresh Memory until it is done (see 00D and 01D of Figure 2-41). Hardware associated with 3000 CPE request is shown in Figure 2-42.

If there is a TV Interrupt, allows Video (TV) Interface TV Memory to fetch new data from Refresh Memory.

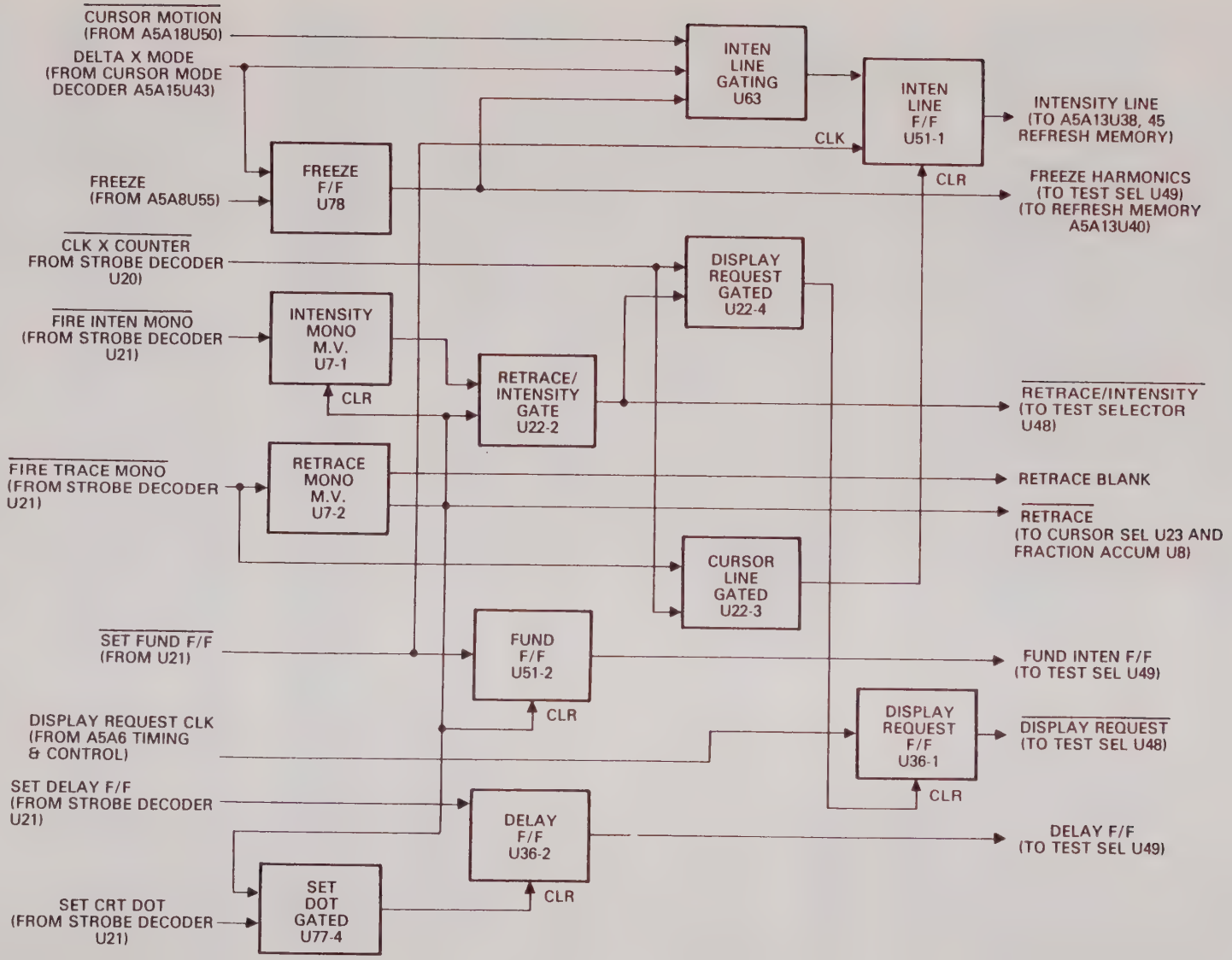
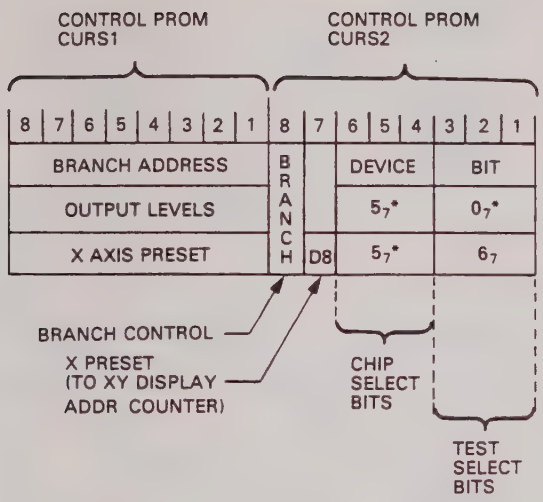

CURSOR MOTION (FROM A5A18U50)
DELTA X MODE (FROM CURSOR MODE DECODER A5A15U43)
INTEN LINE GATING U63
INTEN LINE F/F U51-1
INTENSITY LINE (TO A5A13U38, 45 REFRESH MEMORY)
CLK
CLR
FREEZE (FROM A5A8U55)
FREEZE F/F U78
FREEZE HARMONICS (TO TEST SEL U49) (TO REFRESH MEMORY A5A13U40)
CLK X COUNTER FROM STROBE DECODER U20)
DISPLAY REQUEST GATED U22-4
FIRE INTEN MONO (FROM STROBE DECODER U21)
INTENSITY MONO M.V. U7-1
CLR
RETRACE/ INTENSITY GATE U22-2
RETRACE/INTENSITY (TO TEST SELECTOR U48)
FIRE TRACE MONO (FROM STROBE DECODER U21)
RETRACE MONO M.V. U7-2
RETRACE BLANK
RETRACE (TO CURSOR SEL U23 AND FRACTION ACCUM U8)
CURSOR LINE GATED U22-3
SET FUND F/F (FROM U21)
FUND F/F U51-2
CLR
FUND INTEN F/F (TO TEST SEL U49)
DISPLAY REQUEST CLK (FROM A5A6 TIMING & CONTROL)
DISPLAY REQUEST F/F U36-1
DISPLAY REQUEST (TO TEST SEL U48)
CLR
SET DELAY F/F (FROM STROBE DECODER U21)
DELAY F/F U36-2
DELAY F/F (TO TEST SEL U49)
CLR
SET CRT DOT (FROM STROBE DECODER U21)
SET DOT GATED U77-4

Figure 2-39. Test Selector Input Logic (P/O A5A14 Cursor Control)



*N_x (i.e., 5_7) — integer represents chip selector (U1) output selected, subscript indicates number of selected chip output.

Figure 2-40. Display Control Processor Control PROM (CURS 1, CURS 2) Bit Configuration

If there is a Display Request Clk, the output to display of the next spectral dot is enabled.

If the Integer Countdown Counter has reached zero (INTEGER = 0), Cursor Control Display Control program circuitry will intensify a dot. When Harmonic Cursor is selected, the harmonic dots and line cursor are processed to Refresh Memory by the Control Program Logic.

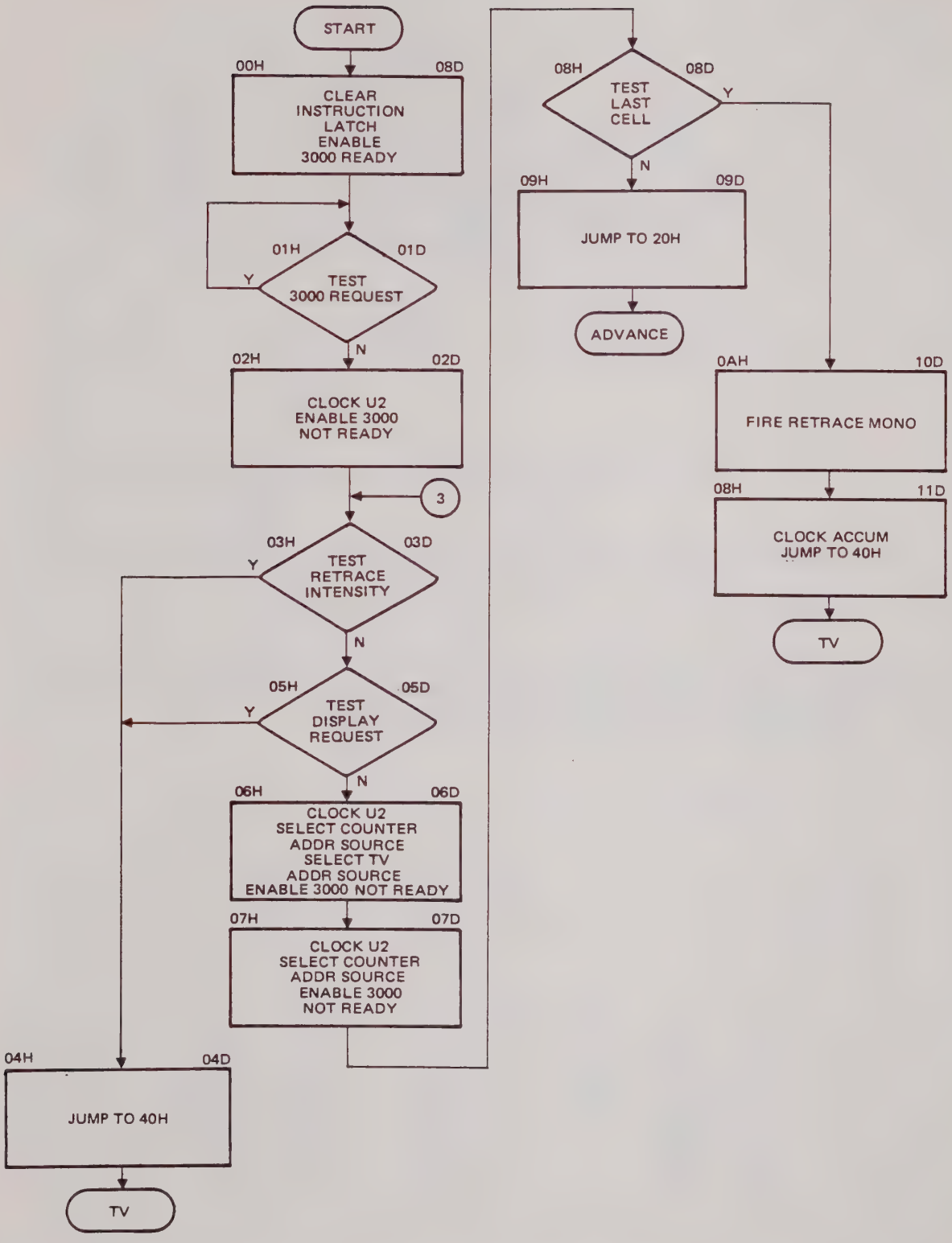


Figure 2-41. Cursor Control (A5A14) Assembly Display Control Program Flow Diagram (Sheet 1 of 5)

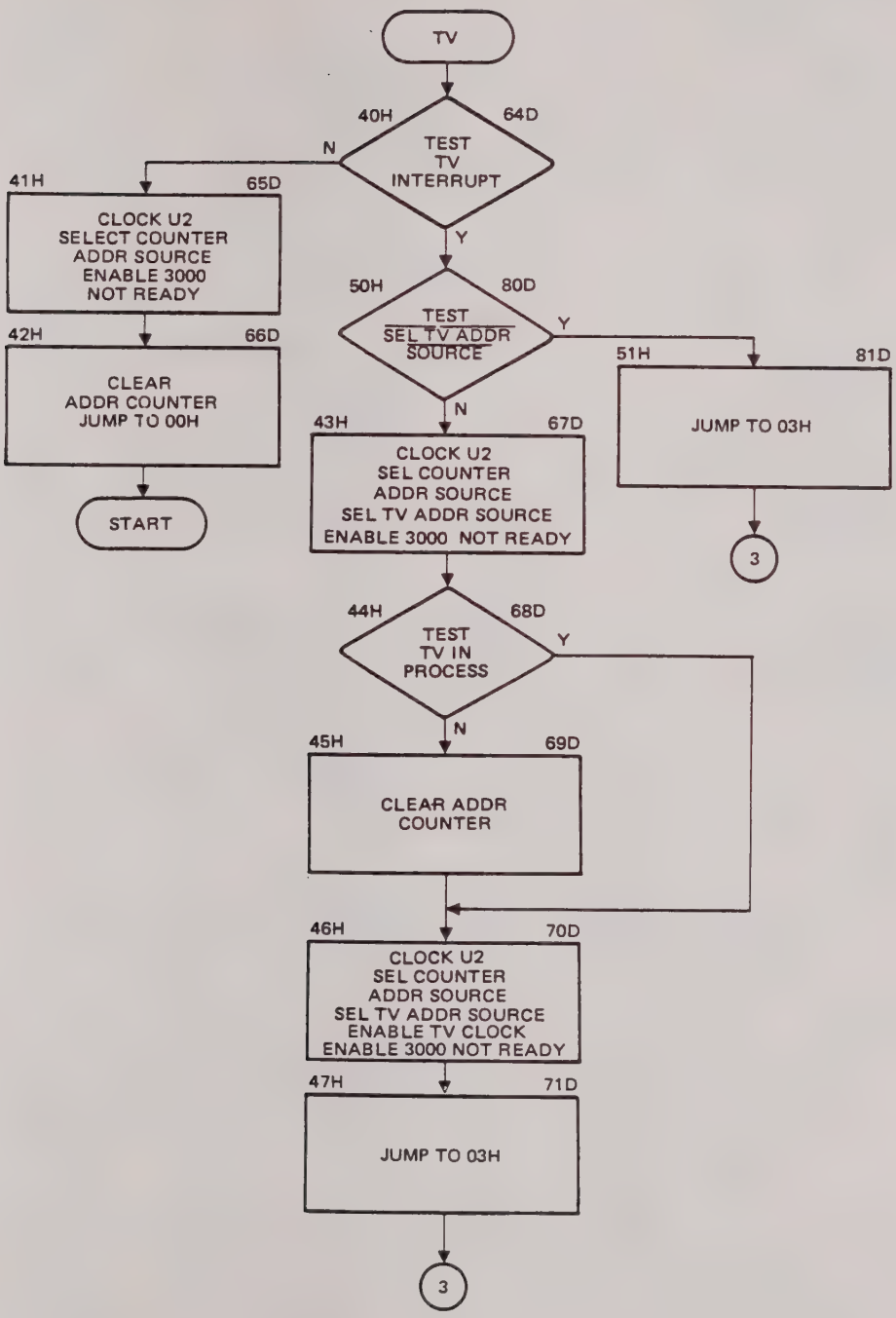


Figure 2-41. Cursor Control (A5A14) Assembly Display Control Program Flow Diagram (Sheet 2 of 5)

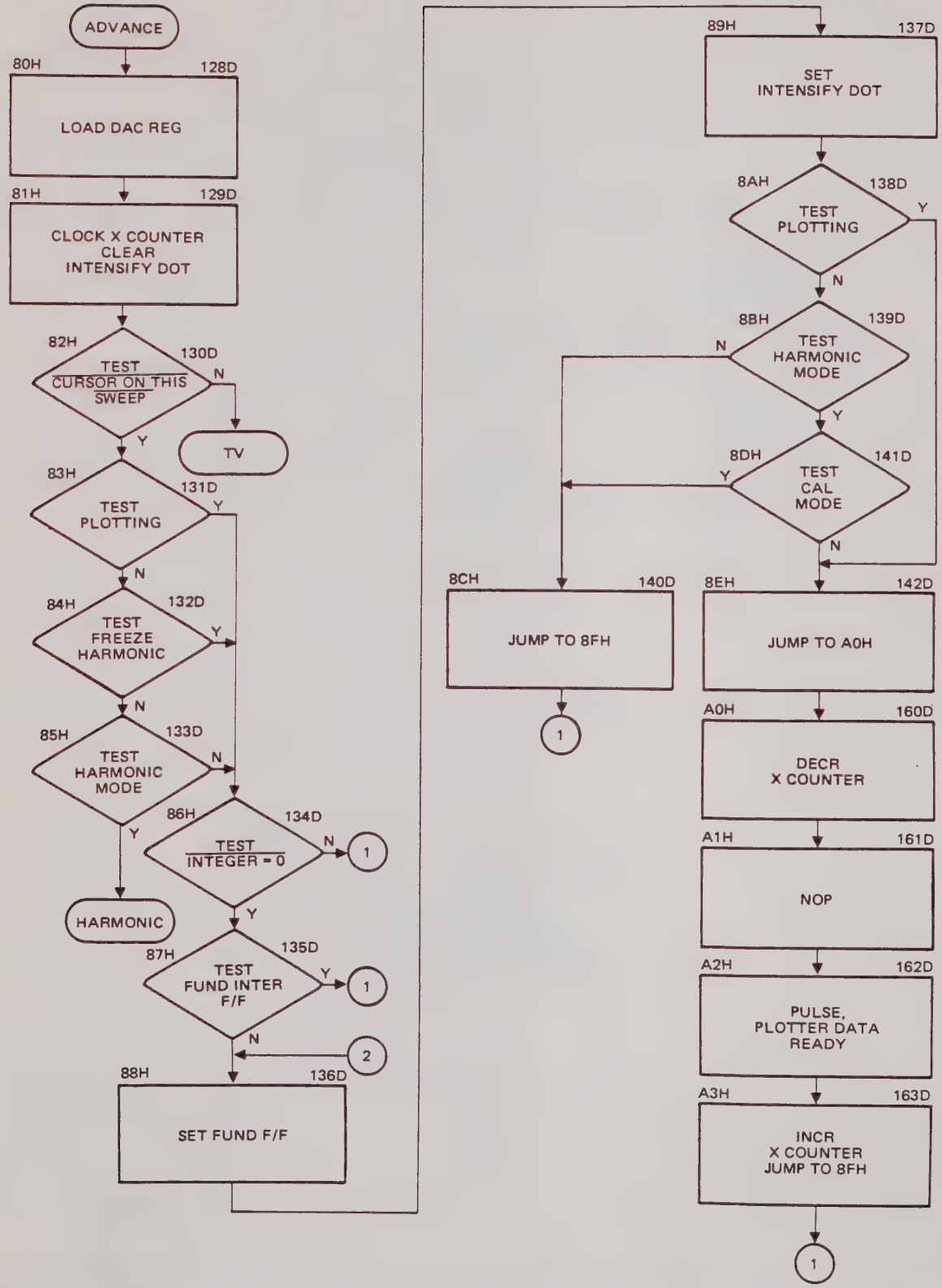


Figure 2-41. Cursor Control (A5A14) Assembly Display Control Program Flow Diagram (Sheet 3 of 5)

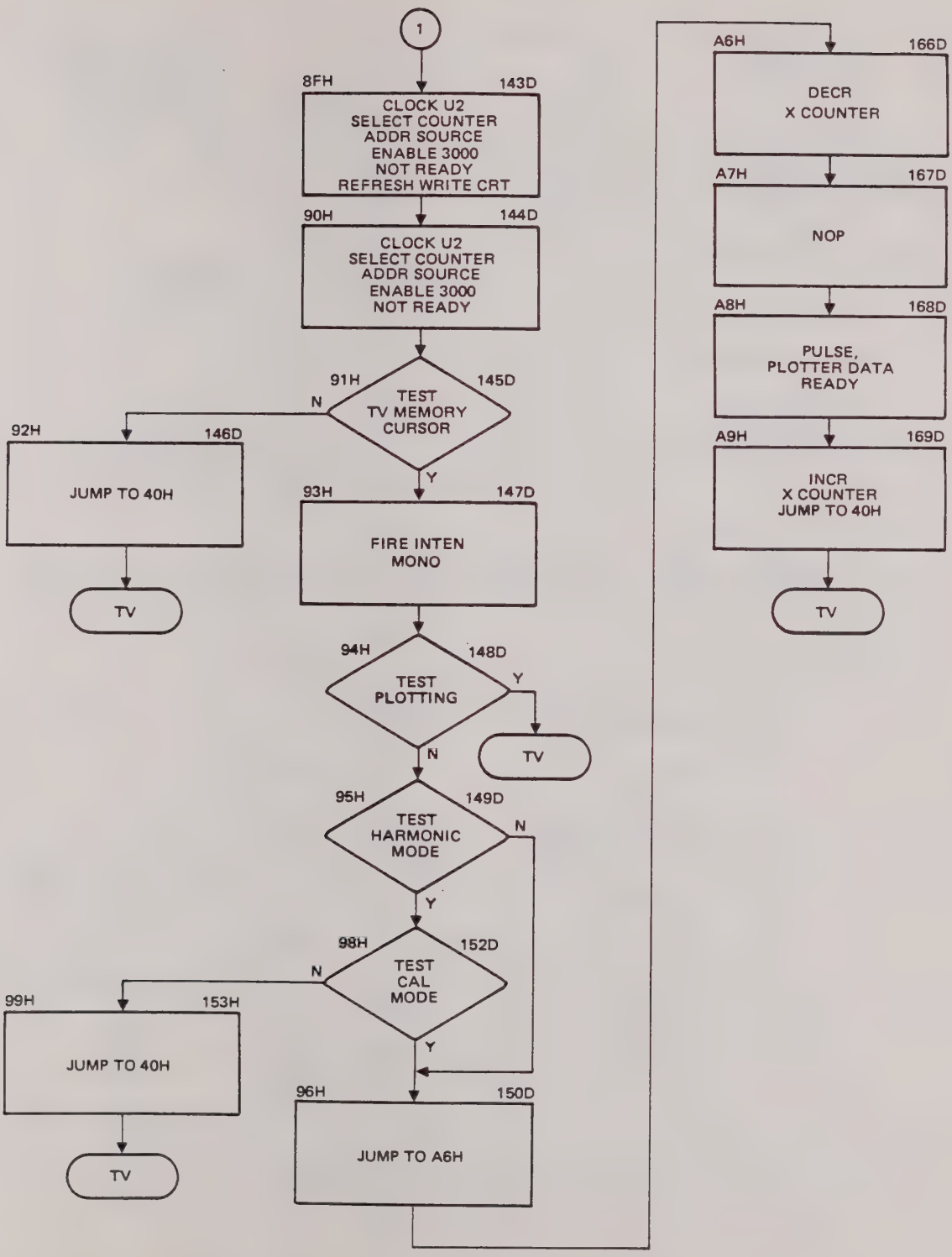


Figure 2-41. Cursor Control (A5A14) Assembly Display Control Program Flow Diagram (Sheet 4 of 5)

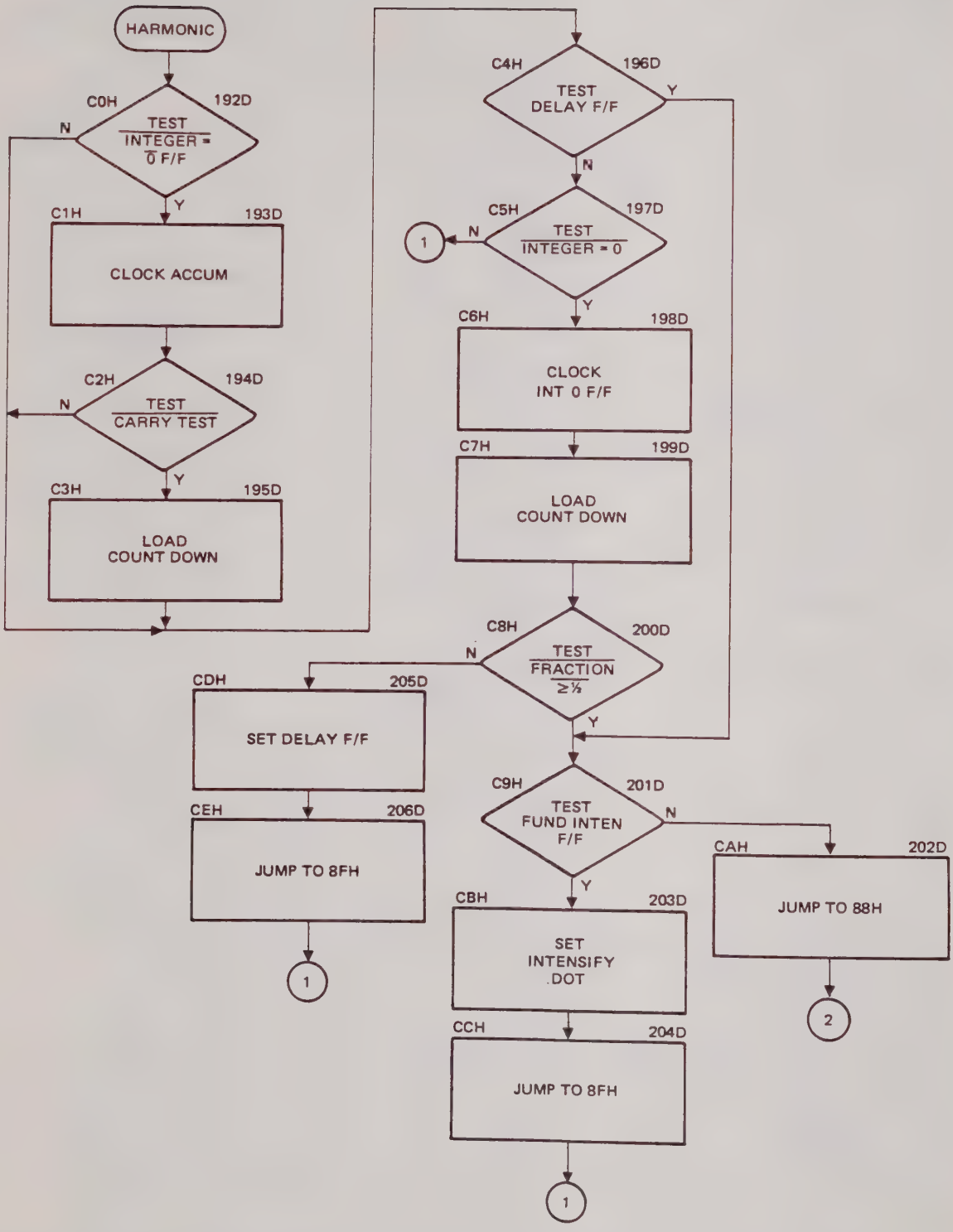


Figure 2-41. Cursor Control (A5A14) Assembly Display Control Program Flow Diagram (Sheet 5 of 5)

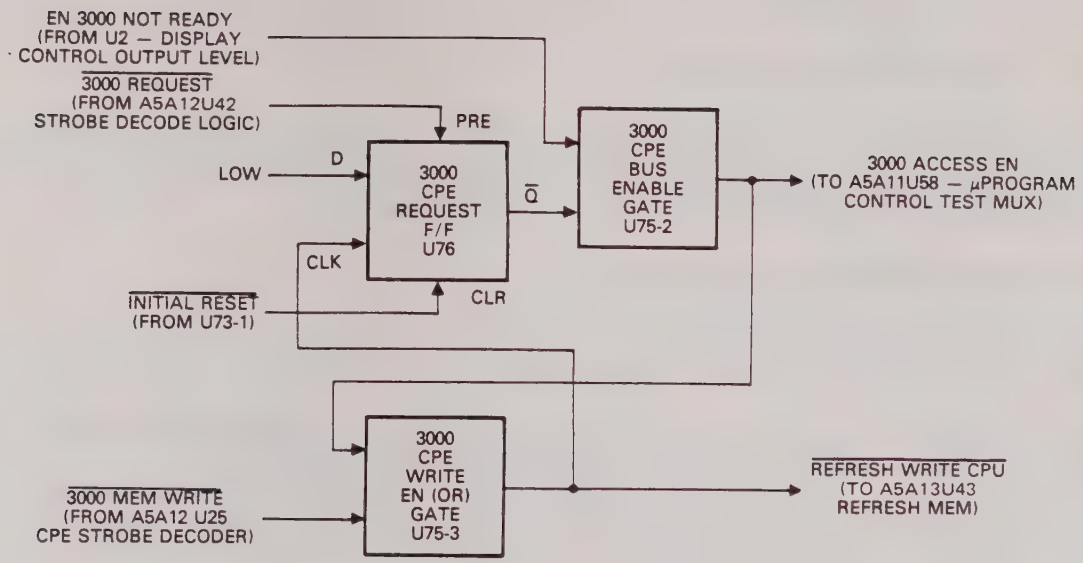


Figure 2-42. Control Circuits for 3000 CPE (Arithmetic Processor)/Refresh Memory Access

2.15.3 Cursor Position Circuitry

2.15.3.1 General

The Cursor Position Circuitry places the cursor on the display at the proper display cell location when in the NORM cursor mode. These circuits also provide harmonics (intensified dots) at all multiples of the fundamental cursor position when in the harmonic (HARM) cursor mode.

2.15.3.2 Cursor Counter Circuits Description

The Cursor Counter Circuitry is simplified in Figure 2-43. A Detailed schematic (drawing number 21084200 Sheet 2) appears in Volume II of this manual.

Initial conditions are established throughout the Cursor Counter Circuitry by INITIAL RESET, CLR CURSOR CNTR, and HARMONIC. These signals clear the Cursor Position Counter (U26, 40, 54) and the Cursor Fraction Counter (U10, 11). HARMONIC (from the Memory Address (A5A15) Cursor Mode Control logic) also clocks the Fundamental Latch (U66, U80) to place data from cursor position and cursor fraction counters on the 3000 Data Bus.

The Control Processor (A5A8) supplied Cursor Left and Cursor Right signals (from Status Logic Output Pulse Decoder U70) to the Cursor Fraction Counter and to the Cursor Position Counter via normal/harmonic select logic (U23, U37). Cursor Right increments these Counters while Cursor Left decrements the Counters.

2.15.4 Normal/Harmonic Cursor Mode Operation

2.15.4.1 Cursor Position Counter

The Cursor Position Counter is loaded with the desired position of the cursor dot. When in the Time Mode, the Z80 Microprocessor places the cursor cell location (1 to 1023) on the Z80 Data Bus and loads the Position Counter with the Z80 LOAD CURSOR*P signal. The Cursor Position Counter is read out to the Z80 Microprocessor via Z80 Data Bus Drivers (U68, 82) which are gated by the Z80 Read Cursor*P signal.

The 3000 CPE reads the Cursor Position Counter via 3000 Data Bus Drivers (U67, 81) which are gated by the Normal Cursor EN signal from the Microprogram Control Assembly (A5A11).

2.15.4.2 Cursor Integer Countdown Counter

The Cursor Integer Countdown Counter (U25, 39, 53) is loaded with the contents (cursor position) of the Cursor Position Counter during retrace time by the LOAD COUNTDOWN signal from the Strobe Decoder U21 (via the NORM/HARM Mode Selector U23). The CLK X COUNTER signal from Display Control Processor Strobe Decoder (U20) decrements the Integer Countdown Counter.

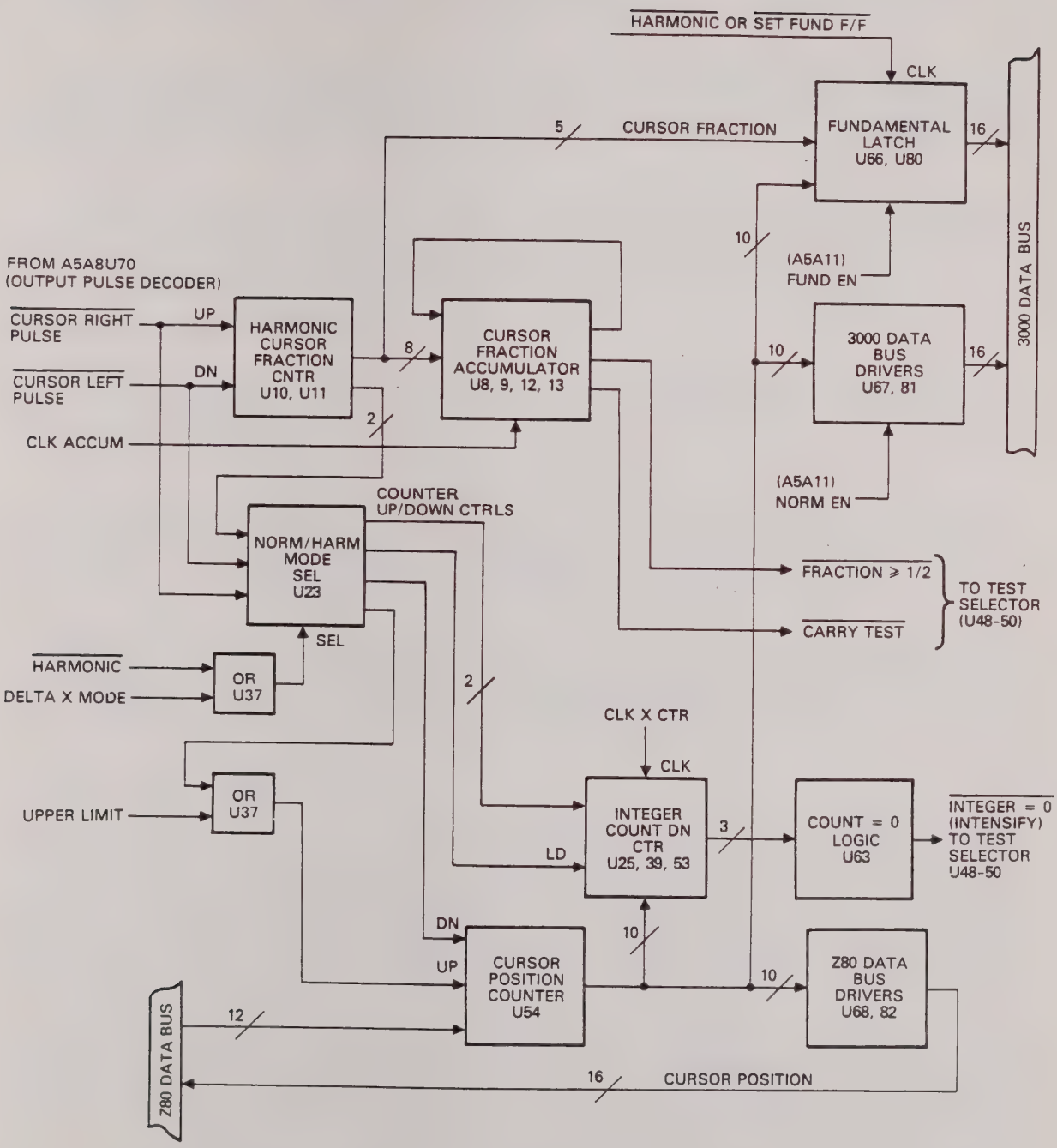


Figure 2-43. Cursor Counter Circuits (P/O Cursor Control Assembly (A5A14)

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When the Cursor Integer Countdown Counter reaches zero (indicating that the cursor position has been reached) the INTEGER = 0 signal is generated by COUNT = 0 Logic (U63) and fed to the INTEGER = 0 flip-flop (U76) and the Test Selector (U48-50).

These signals, when active, result in CLK INT 0 FF being decoded by Display Control Processor and fed to (U76). The intensified dot cursor is stored in Refresh Memory at the memory location which corresponds to the output of the Cursor Position Counter as read by the 3000 CPE via the 3000 Data Bus Drivers (U67, 81) to A5A13 U34, and U51.

For harmonic cursors (HARM mode), the Cursor Integer Countdown Counter is reloaded with the contents of the Cursor Position Counter each time it reaches zero. The cycle described above is repeated to place equally spaced intensified dots at all harmonics of the fundamental cursor location.

2.15.4.3 Harmonic Cursor Fraction Counter

The Harmonic Cursor Fraction Counter (U10, 11) provides an extended (fractional) precision of the normal cursor for the harmonic cursor mode. This allows the fractional resolution of cursor positions between adjacent fundamental cell locations.

The Harmonic Cursor Fraction Counter supplies five (5) additional low order bits with the Cursor Position to the Arithmetic Processor (A5A12) via the Fundamental Latch. The Harmonic fraction and the fundamental cursor position information are then used by the 3000 CPE to compute orders of the cursor location.

The Cursor Fraction Counter also supplies cascading inputs to the Cursor Position Counter via the NORM/HAR Mode Selector (U23). This effectively increases the size of the Cursor Position Counter by 8 bits (from 12 to 20 bits). The fraction counter counts between 0 and 1 in 256 steps (1/256) while the integer counter counts between 1 and 408 (spectrum mode) in one count steps.

2.15.4.4 Cursor Fraction Accumulator

The Cursor Fraction Accumulator (U8, 9, 12, 13) is operable during harmonic cursor operations to let the Display Control Processor know when to (1) load and count the Cursor Integer Counter down and (2) position the dot if the cursor is between Integer cell locations. When an intensified dot is generated, the count in the Harmonic Cursor Fraction Counter is added to the contents of the Fraction Accumulator. When an overload is generated (CARRY TEST), the Cursor Integer Counter (U25, 39, 53) is decremented by CLK X COUNTER signal via the Display Control Processor.

If the cursor is between adjacent fundamental cell locations (a fractional count between 0 and 1 on the Harmonic Cursor Fraction Counter), the intensified dot position is determined by the FRACTION $\geq$ ½ signal. The fraction accumulator generates this signal when its stored count reaches 80_H (128_D). This tells the Display Control Processor to position the intensified dot at the next whole (integer) cell location.

In order to generate fixed harmonic dots, intensified dots are written into Refresh Memory via A5A14 U78 (see Figure 2-39 Test Selector Input Logic).

2.15.5 Display Mode Decoding and Control

2.15.5.1 Display Request

The Display Control Processor (DCP) allows intensified dots to be generated as long as DISPLAY REQUEST is held low by a high level at U36–1 (see Figure 2-39 Test Selector Input Logic). This level tells the DCP that there is time for one more X-Y Dot. The Display Request flip-flop (U36–1) is cleared at the end of the X-Y sweep by U22–4.

2.15.5.2 Display Mode Decoding

The 3-bit Display Mode is supplied to Display Mode Decoding and Control circuitry (shown in Figure 2-44) from the Front Panel Interface (A5A18) Assembly and latched into the Display Mode Latch (U65) by 10 Hz CLK. The Display Mode Decoder (U64) provides the following outputs.

Display Mode Decoder Inputs	Display Mode Decoded
000	SPECTRUM
001	TIME
010	DUAL SPECTRUM
011	TIME SPECTRUM
100	DUAL TIME
101	CO-QUAD

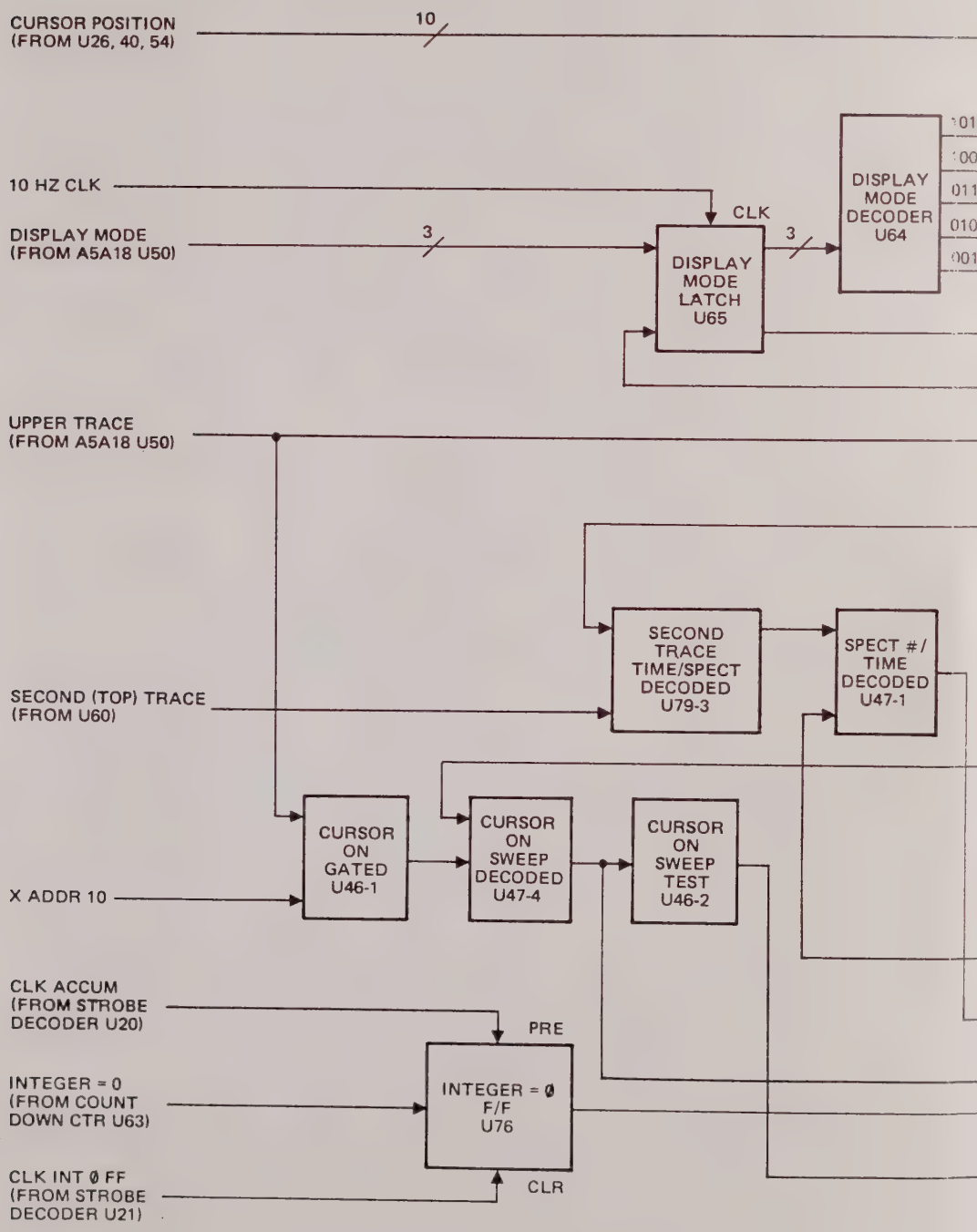
The above decoded display modes provide controls for various system functions associated with them as indicated in the display mode decoding and control functional block diagram (Figure 2-44).

2.15.5.3 Display Time Control

The Cursor Position Comparator (U41, 59, 83) functions to (1) indicate when the cursor has reached its upper limit and (2) to reset (CLEAR) the position counter when it exceeds the upper limit.

When spectrum displays are decoded by the Display Mode Decoder, the Comparator compares the binary code (400_D) its B inputs to the count stored by the Cursor Position Counter. When the Cursor position is equal to 400 (cell 400) the Comparator provides an A = B output (Upper Limit) to the Cursor Position Counter U54 (via U37) which clocks the Cursor Position Counter up once more to generate a stored count of 401. The Cursor Position Comparator then produces A > B. The A > B pulse is fed to the Display Mode Latch (U65). The latch output is a high level (Reset Cursor) to clear the Cursor Position Counter.

When Time displays are decoded (i.e., Time, Dual Time, Time and Spectrum), the Dual/Upper Trace Decoded (U62, 77–2) and the Time/Dual Time/Spectrum-Time (U61–1) gates supply the 10-bit binary coded upper limit input (B) to the Cursor Position Comparator. This count is 1023_D. The Cursor Comparator will function as described above when cell 1023 is reached and exceeded.


CURSOR POSITION
(FROM U26, 40, 54)
10
10 HZ CLK
DISPLAY MODE
(FROM A5A18 U50)
3
CLK
DISPLAY
MODE
LATCH
U65
3
DISPLAY
MODE
DECODER
U64
UPPER TRACE
(FROM A5A18 U50)
SECOND (TOP) TRACE
(FROM U60)
SECOND
TRACE
TIME/SPECT
DECODED
U79-3
SPECT #/
TIME
DECODED
U47-1
X ADDR 10
CURSOR
ON
GATED
U46-1
CURSOR
ON
SWEEP
DECODED
U47-4
CURSOR
ON
SWEEP
TEST
U46-2
CLK ACCUM
(FROM STROBE
DECODER U20)
PRE
INTEGER = 0
(FROM COUNT
DOWN CTR U63)
INTEGER = Ø
F/F
U76
CLK INT Ø FF
(FROM STROBE
DECODER U21)
CLR

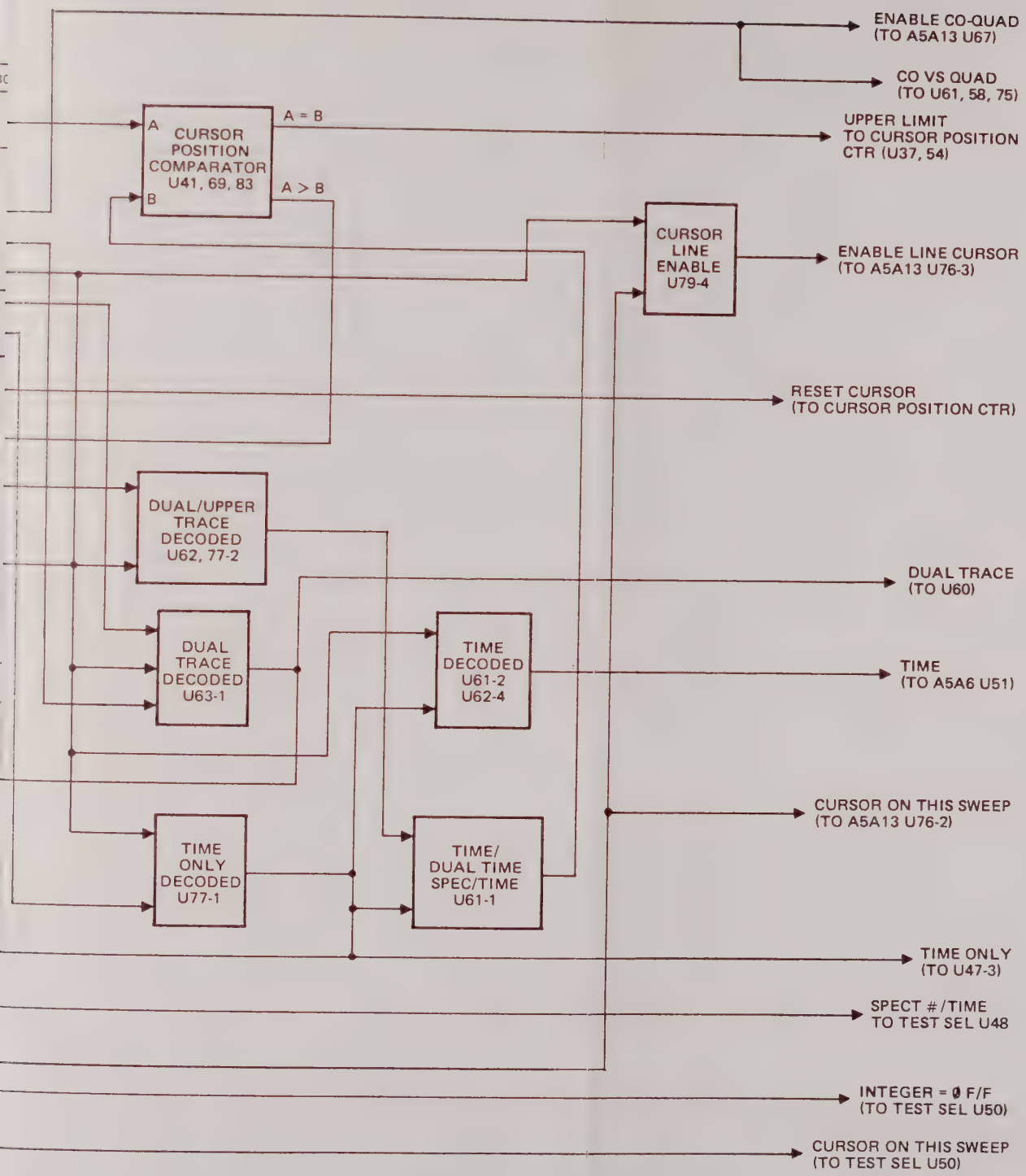


Figure 2-44. Display Mode Decoding and Control (P/O A5A14 Cursor Control Assembly)

2.15.6 Transfer Control Logic

2.15.6.1 General

Transfer Control Logic performs the functions of (1) transferring Refresh Memory data to the Video Interface Assembly (A5A16) TV Memory, (2) decoding display mode and 3000 CPE Address Bus inputs to allow for dual-trace data transfer operations, and (3) providing a digital X-sweep and Memory Address source for an external X-Y scope. Transfer Control Logic is composed of the TV Transfer Controller and Two-Trace Transfer Logic (shown in Figure 2-45). The TV Transfer Address Counter, The X-Y Display Address Counter, Trace Select circuitry, and the TV Address Source Selector (shown in Figure 2-46) are also part of the Transfer Control circuitry.

2.15.6.2 TV Transfer Controller

The TV Transfer Controller is driven by the 4.096 MHz Clock Generator (U74, U46). The high level (ENABLE TV CLOCK) from the Display Control Processor (U2) allows the clock signal to appear at the TV XFR Counter (U42) clock up input.

The TV XFR Counter provides four address bits for the TV XFR Microprogram Instruction PROM (U43). When either of the three time display modes are decoded, the Time Display Logic (U47, 75–4) provides the high order (2^4) bit to access the time transfer instruction subroutine. The instruction PROM outputs are latched with the 4 MHz clock fed to the TV XFR Instruction Register (U44).

The TV Transfer Controller feeds Clock pulses to the TV Transfer Address Counter (U6, 19, 33 of Figure 2-46). The TV Transfer Address Counter supplies address information to cause a high-speed *retrace time* read of Refresh Memory data to the TV Memory on A5A16 (Video Interface Assembly).

2.15.6.3 TWO-TRACE Transfer Logic

The TWO-TRACE Transfer Logic (shown in Figure 2-45) uses the Select Refresh A and B signals from Processor Memory (A5A13) Chip Select Logic and the LD DATA READY signal from the 3000 CPE Strobe Decoder to signal the Display Control Processor that the 3000 CPE has new data available to store in Refresh Memory.

The two primary outputs from TWO-TRACE Transfer Logic are TV INTERRUPT and TV IN PROCESS. The TV INTERRUPT signal tells the Display Control Processor (DCP) that Refresh Memory Data is to be transferred to the TV memory on A5A16. TV IN PROCESS tells the DSP that the TV Transfer Address Counter (U6, 19, 33) has been cleared and that the data transfer is in process under the direction of the TV Transfer Controller.

Initial conditions are established by LD DATA READY or Select Refresh A or Select Refresh B. Either of these signals will set U70–1 or U70–2 (Upper and Lower Transfer Set F/Fs). The TV INT GATE (U72) output (TV INTERRUPT) level is held low by the complemented outputs of XFR UPPER and LOWER F/F's (U56–1, U56–2).

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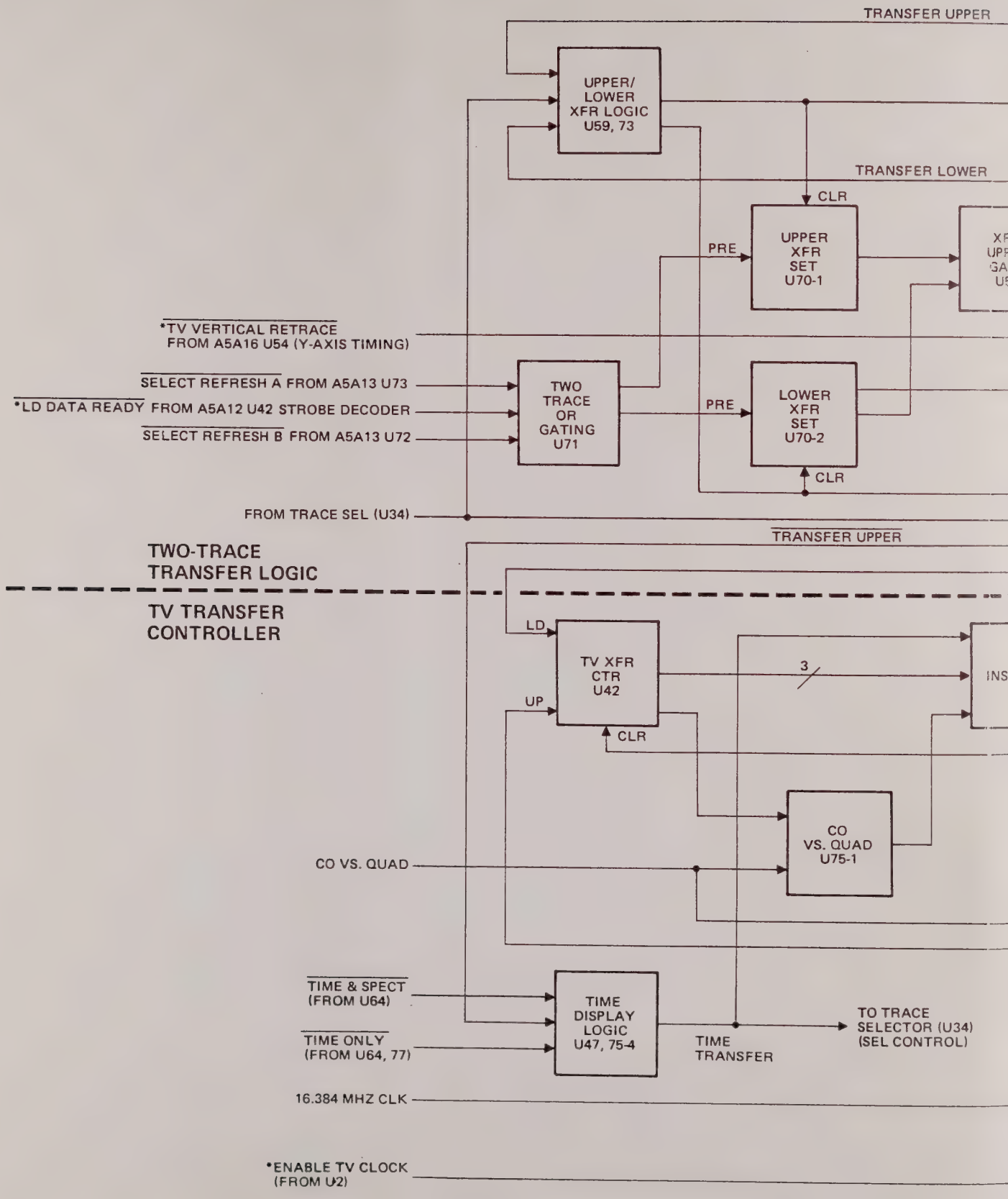
TRANSFER UPPER
UPPER/
LOWER
XFR LOGIC
U59, 73
TRANSFER LOWER
CLR
PRE
UPPER
XFR
SET
U70-1
*TV VERTICAL RETRACE
FROM A5A16 U54 (Y-AXIS TIMING)
SELECT REFRESH A FROM A5A13 U73
*LD DATA READY FROM A5A12 U42 STROBE DECODER
SELECT REFRESH B FROM A5A13 U72
TWO
TRACE
OR
GATING
U71
PRE
LOWER
XFR
SET
U70-2
CLR
FROM TRACE SEL (U34)
TRANSFER UPPER
TWO-TRACE
TRANSFER LOGIC
TV TRANSFER
CONTROLLER
LD
TV XFR
CTR
U42
3
UP
CLR
CO
VS. QUAD
U75-1
CO VS. QUAD
TIME & SPECT
(FROM U64)
TIME ONLY
(FROM U64, 77)
TIME
DISPLAY
LOGIC
U47, 75-4
TIME
TRANSFER
TO TRACE
SELECTOR (U34)
(SEL CONTROL)
16.384 MHZ CLK
*ENABLE TV CLOCK
(FROM U2)

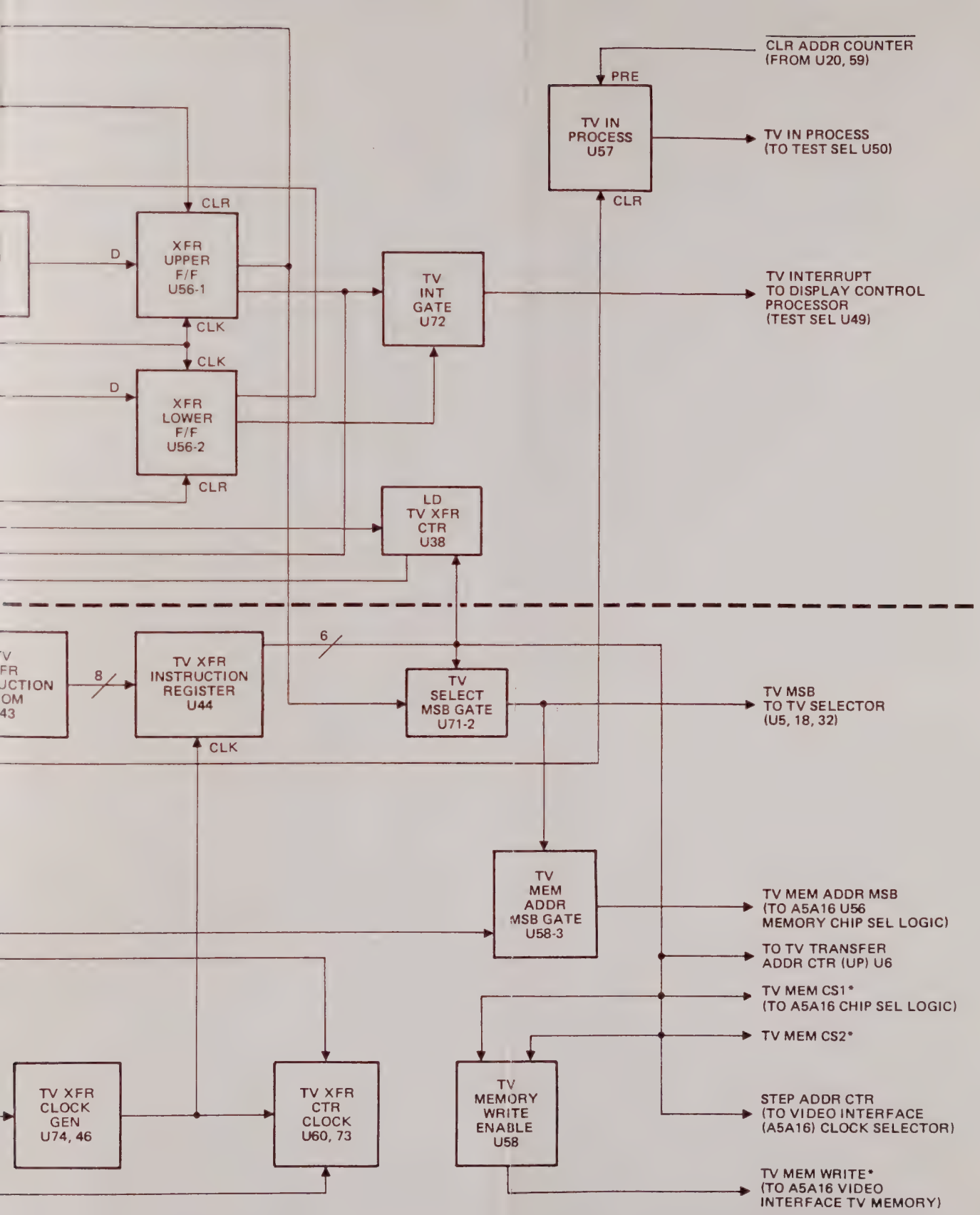

Figure 2-45. TV Transfer Control Logic (P/O A5A14 — Cursor Control)

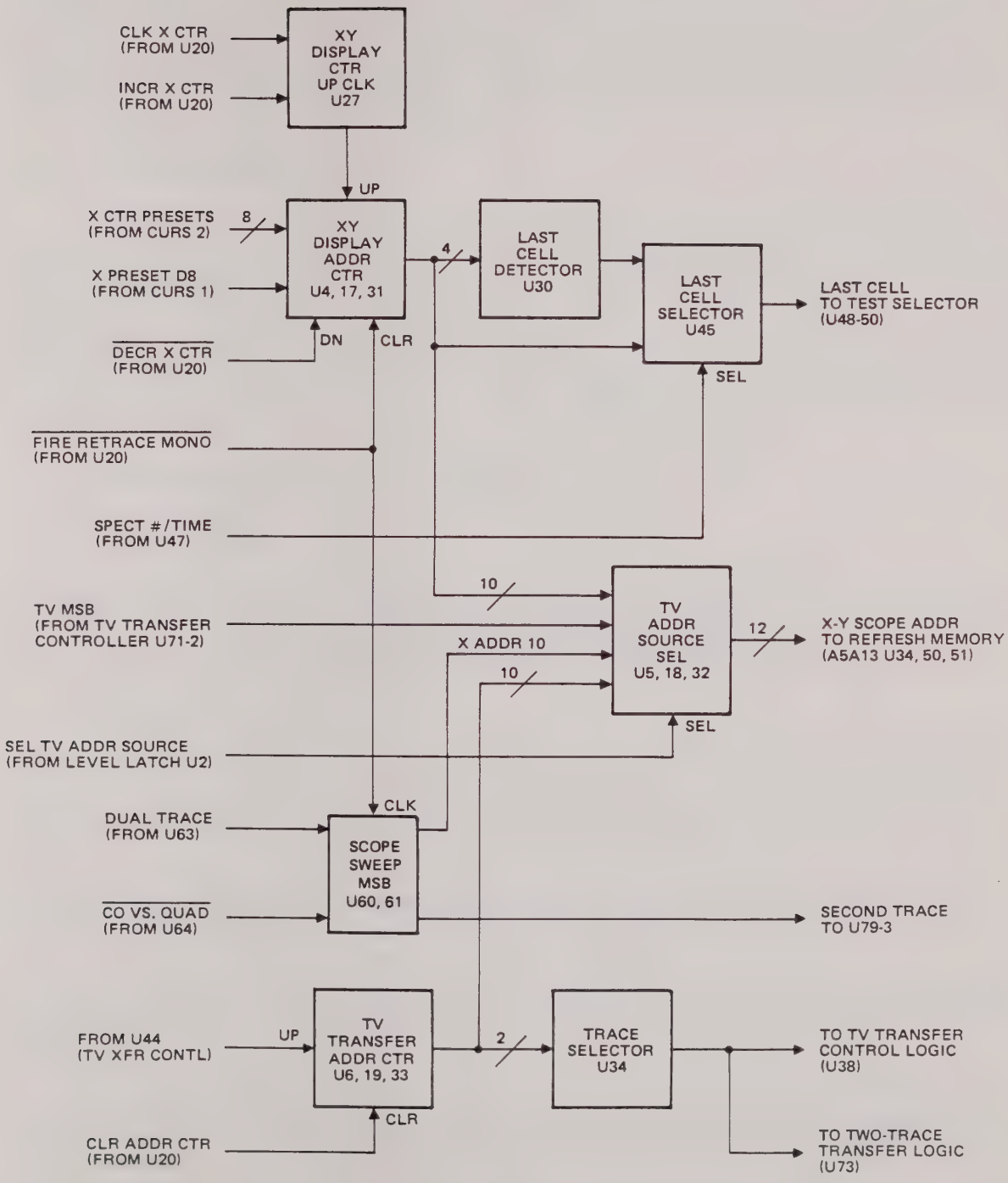

Figure 2-46. Simplified Block Diagram X-Y Display/TV Transfer Address Counters and Trace Select Circuitry (P/O A5A14 — Cursor Control)

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The MSB of the TV Transfer Address Counter (U6, 19, 33) is fed to the Upper/Lower XFR Logic (U59, 73) via Trace Selector (U34). The presence of the MSB tells the TWO-TRACE Transfer Circuitry that there are two channels of data and causes the logic to complement the states of the XFR UPPER and LOWER flip-flops (U56 -1 and -2). The above described circuit operation allows the transfer of lower trace data to proceed when the transfer of upper trace data has been completed.

2.15.6.4 X-Y Display Address Counter

The X-Y Display Address Counter (U4, 17, 31, shown in Figure 2-46) serves as an X sweep and Memory Addressing source for an external X-Y SCOPE. It also provides inputs to the Last Cell Detector (U30). When the last cell of either a Spectrum (cell 404) or Time (1024) Mode Display is completed, the Last Cell Detector or the X-Y Display Counter (X_{10} bit) is selected by the Last Cell Selector (U45) as the Last Cell signal and fed to the Display Control Processor Test Selector (U48). When tested, the DSP generates the FIRE RETRACE MONO strobe which clears the X-Y Display Address Counter, triggers the Retrace Multivibrator (U7) which provides an external X-Y blanking signal and disables the X ADDR 10 bit to Display Mode Decoding and Control (U46-1 *Cursor On* GATED) which disables the line cursor.

2.16 PLOTTER CIRCUITS DETAILED DESCRIPTION

2.16.1 General Description

The plotter circuitry is contained on the Low Pass Filter and Plotter Assembly (A5A3) and supplies analog X-axis and Y-axis signals to the rear panel for an external analog plotter. The plotter output circuitry is illustrated in Figure 2-47 and Sheet 4 of drawing number 21232500 (Volume II).

2.16.2 Plotter Output Circuitry

The EN PLOTTER X, EN PLOTTER Y, Z80 I/O READ, and Z80 I/O WRITE signals are generated by the Control Processor and fed to (1) the Processor Memory (Refresh) in order to read the horizontal and vertical data and (2) write that data from the Z80 Data Bus into the X-Latch (U29, 30) and Y-LATCH (U35, 36).

Refresh Memory Data words are clocked into the plotter output circuit X and Y Latches by the PLOTTER DATA READY strobe from the Cursor Control Assembly.

The X and Y Latches feed the 12-bit digital horizontal and vertical data words to the X-DAC (U28) and Y-DAC (U34) respectively. The digital data words are converted to analog voltages and fed to amplifiers U26 and U32.

The X Plotter signal is fed to rear panel connector (J10). Y Plotter data from amplifier U32 is fed to the front panel Gain Vernier and Offset Control and amplified by U27 and U25 before being applied to rear panel connector (J11).

Amplifier U31 is employed to reduce the nonlinearity in the converted signals that would result from the imprecise amplitudes of the input digital signals on each DAC. U31 maintains a constant reference voltage to both DAC assemblies and thereby eliminate the effects of environmental and DAC ladder load resistance variations on the analog outputs generated.

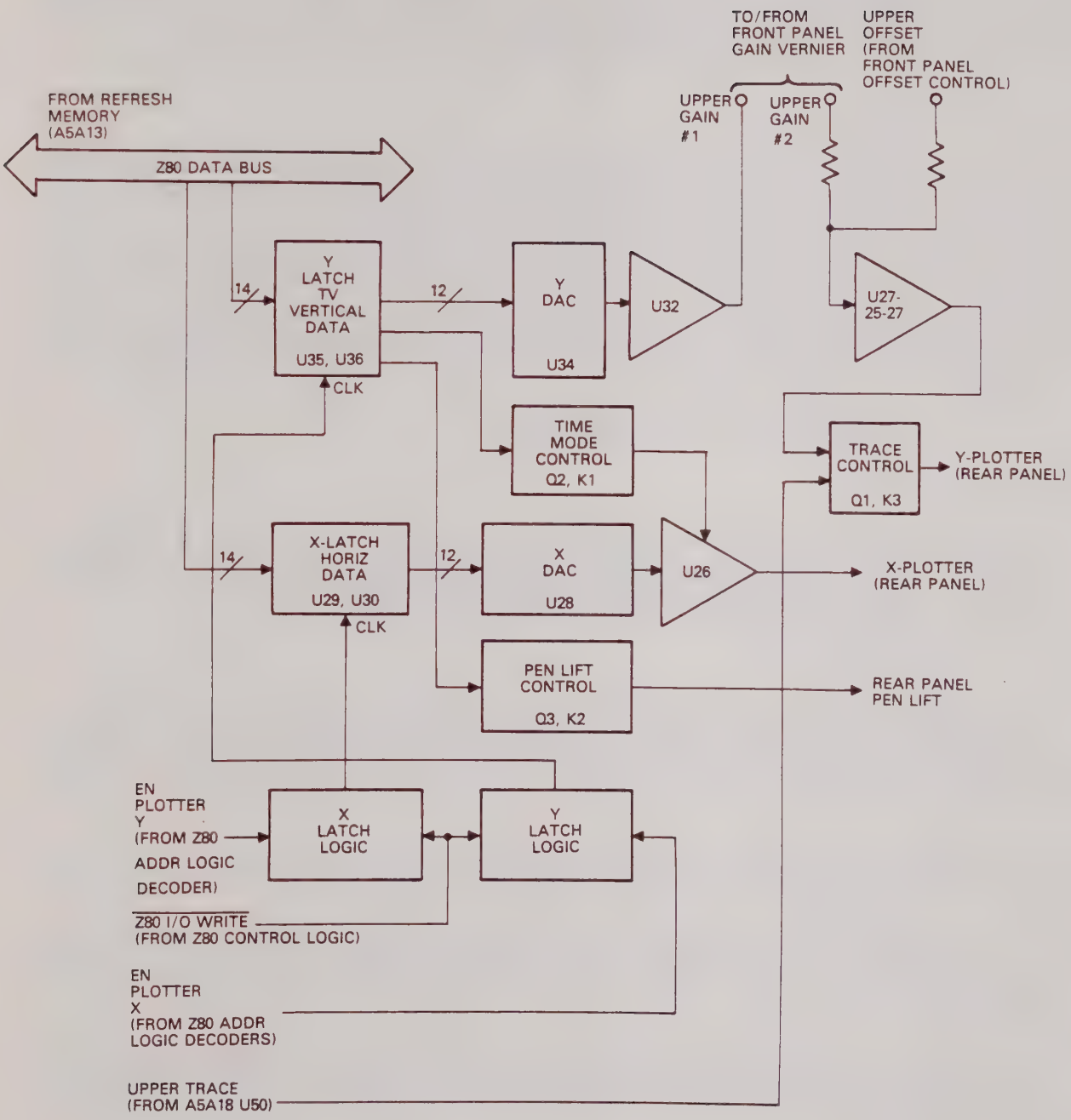


Figure 2-47. Plotter Output Circuits (P/O A5A3 Assembly)

2.17 POWER SUPPLY

2.17.1 General Description

The Power Supply is comprised of three (3) major circuit groups:

Power Panel (PS1A3)
Inverter (PS1A2)
Regulator (PS1A1)

The following discussion of the Power Supply will refer to Figure 2-48 (Power Supply Simplified Block Diagram) and Schematic Drawings 21240600 (Sheets 2 and 3) when references to circuit components are made.

The Power Panel Assembly contains primary input fusing, switched rectification, and filtering circuitry to bias the inverter assembly.

The Inverter Assembly contains supply voltage generation and control circuits, power failure interrupt circuits, over voltage protection circuits, and power supply regulators.

The Regulator Assembly contains rectification circuits for regulating Inverter inputs and supplies regulated +12V, +15, −15, +5V regulated outputs to the circuits contained in the SD375.

2.17.2 Power Panel Assembly

Primary power is fed to T1 (see Schematic Sheet 2) when the Power On switch is depressed. T1, CR1 are configured as a full wave doubler to develop Collector supply voltage for the operation of the Oscillator Output Amplifiers PS1A2 Q1 and Q2.

Primary input power is also fed to the Inverter Assembly (PS1A2) via P3/J3 pins 1, 8, and 4.

On the Inverter assembly (PS1A2), RT1 and RT2 are connected across the bridge rectifier CR1 as surge limiting thermistors to reduce power up surges through CR1. DS2 is a neon relaxation oscillator to indicate to the technician that high voltage is present.

DS1 provides protection if the instrument is erroneously supplied 200 Vac when configured for 100 Vac operation. This configuration merely results in blowing F1 (the 10 amp primary power fuse).

2.17.3 Inverter Assembly

The primary function of the Inverter Assembly (PS1A2) is to control the operation of the high frequency power switches Q1 and Q2 and thereby provide a stable Alternating Current Source for the +12, +15, +5, and −15 volt power supplies. It accomplishes this by monitoring the regulated outputs from the regulator assembly (PS1A1) to detect load variations, overvoltage surges, and power failures.

From the Power Panel Assembly, primary power is fed via T2 through J37-8 to CR19 (a single phase full wave bridge rectifier). Its rectified output is regulated at +12 volts by U3.

2.17.4 Current Limiting Circuit

The high speed op-amp PS1A2 U1 (Schematic Sheet 2) is employed to control the high frequency switching during startup to insure a soft start. This is accomplished through Q3 and Q4 by keeping the duty cycle of the Pulse Width Modulator low during power up to reduce stress on switches Q1 and Q2.

T3 senses changes in current drain to PS1A3 T1 and the primary power source. The full wave bridge across its secondary feeds these changes to U1. An increase in T3 primary current results in the U1 output level going low and Q3 collector going high to Q4. This results in increasing the supply voltage that is used to charge C19 and thereby lowering the duty cycle of the Modulator.

2.17.5 High Frequency Oscillator

The high frequency oscillator (PS1A2 U4) was employed as an alternating current power source in order to provide the greatest isolation from and/or eliminate signal frequency components in the pass band of the Dynamic Analyzer II. The use of conventional line voltages could result in measurement errors due to ripple at frequencies within the passband of the instrument.

U4 is a square wave oscillator whose output frequency is approximately 52 KHz. The duty cycle of this 52 KHz square wave is varied by controlling the bias on Schmitt Trigger (U4C).

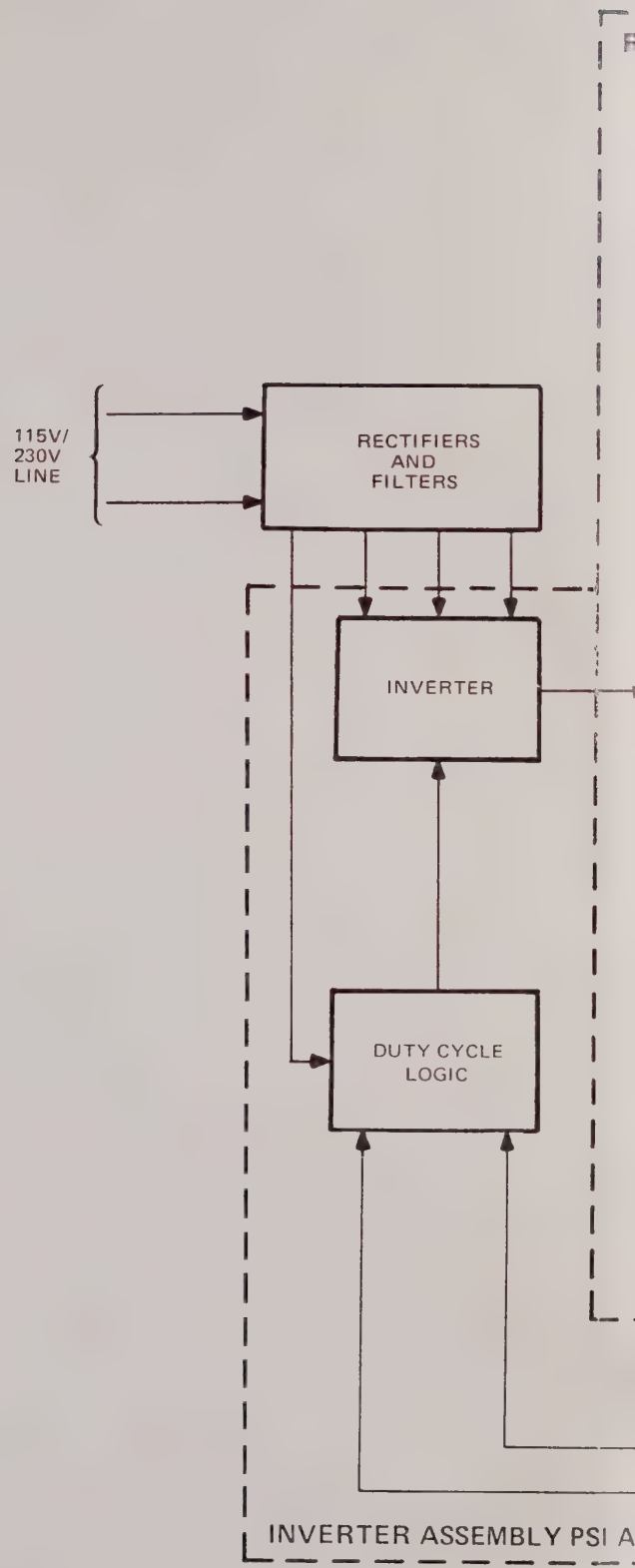
By varying the duty cycle, the amount of power in the square wave (its average value) is increased or decreased in direct proportion to duty cycle.

This principle is used to maintain a stable alternating current supply to the Regulator Assembly.

Control of the duty cycle is accomplished using Q4–C which is biased by the Current Limit Circuit U1, Q3. The voltage on Q4–C increases or decreases to charge the threshold (crossover) potential of Schmitt Trigger inverter U4–B. The capacitor (C–19) requires more time to charge to a higher potential and less time to charge to a lower potential (threshold).

2.17.6 Steering Logic and Power Drivers

The output of the oscillator is fed to U5–8 and gated to U5–A and U5–B via inverter U5–11. U5A and B feed the push pull operated Darlington Drivers which are connected to the primary of T1. U5–A and B are alternately enabled by flip-flop U6. U6 is clocked by the oscillator and its outputs (Q and $\overline{Q}$) alternately place high (enabling) levels on D gates U5–A and B. The asymmetrical output from the oscillator to each gate controls the amount of time that current flows through both halves of transformer T1's primary from either of the two Darlington Power Drivers.


115V/
230V
LINE
RECTIFIERS
AND
FILTERS
INVERTER
DUTY CYCLE
LOGIC
INVERTER ASSEMBLY PSI A

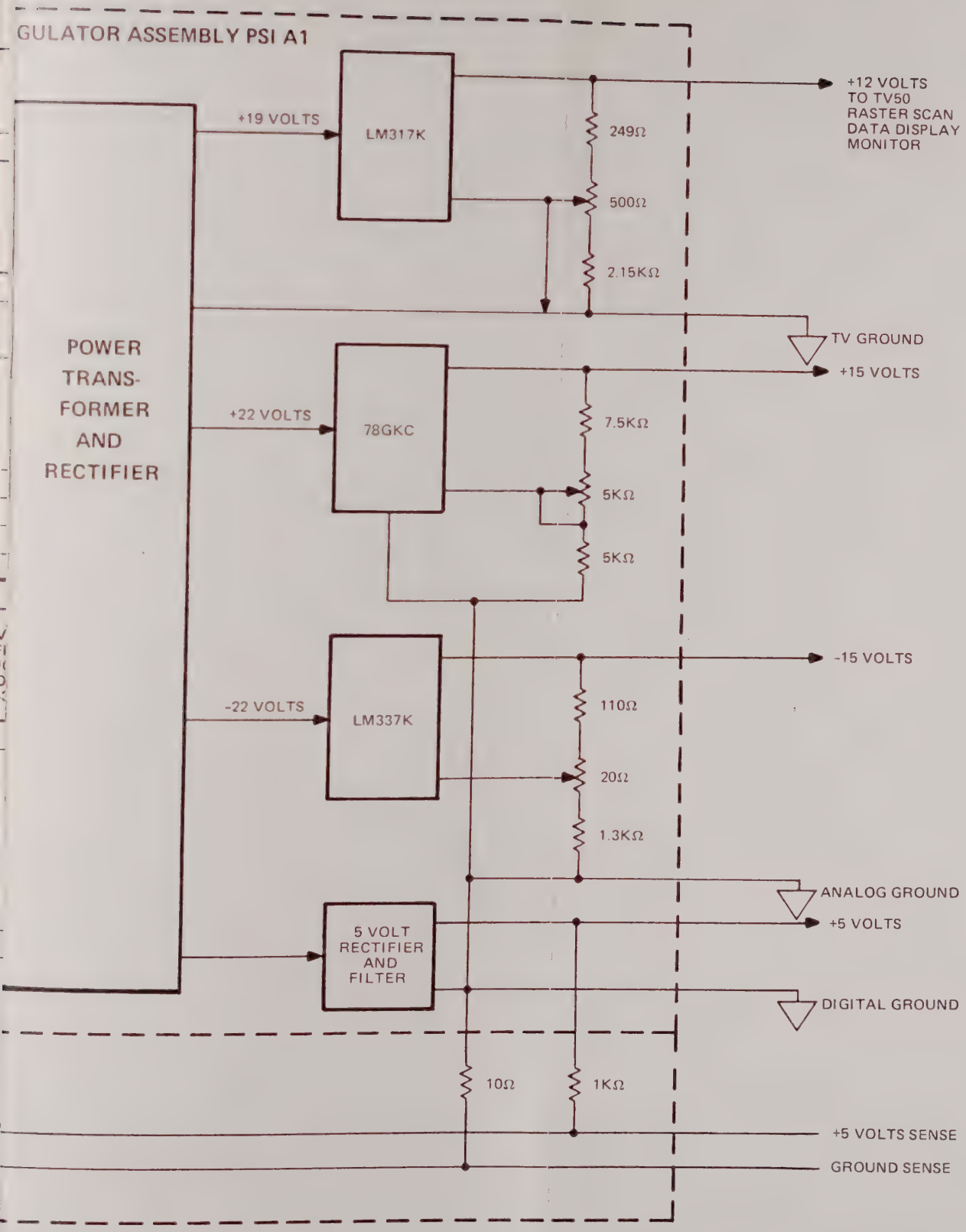


Figure 2-48. Power Supply, PS1 Simplified Block Diagram

2.17.7 High Voltage Switching

The High Voltage Switch (consisting of Q1, Q2 and T1 and the other peripheral components) is bias between the +150 volts and C1, R1 when Q1 conducts and the −150 volts on C2, R2 when Q2 conducts through the primary power return.

Q1 and Q2 are alternately switched on and off and the common emitter collector swings between +150 and −150 volts. The current path for the Darlington Drives is switched on and off but is on only during the periods when transformer T1 primary current is flowing. This reduces power consumption, eliminates oscillating induced secondary to primary voltages, and makes for a more efficient power supply.

2.17.8 Regulator Assembly

The output of the High Frequency Power Switch is transformer coupled to the regulation circuitry on PS1A1 (Schematic Sheet 3).

The transformer (PS1A1T1) secondary is connected to four full wave bridge networks to develop the unregulated DC voltages required to provide +12, ±15, and +5 volt regulated outputs.

The +15 and −15 volt regulators are contained on positive and negative adjustable IC voltage regulators U2 and U3 respectively.

Regulator PS1A1 U1 is a series connected adjustable regulator for the +12 volts supplied to the Data Display Monitor (TV 50). All other voltages required by the crt are internally generated. Refer to Appendix A for details on the Data Display Monitor.

2.17.9 5 Volt Supply

The Rectifier Assembly is connected to the six secondary windings on PS1A1 T1 and supplies the unregulated DC voltage for the regulated +5 volts. The unregulated output is filtered by L1, L2, L3, R10, and capacitors C13 through C17.

Regulation of the +5 volts is accomplished by shunt regulator PS1A2 U2 on the Inverter Assembly.

2.17.10 Overvoltage Protection

Overvoltage protection is provided by Q6, Q5, and U5-C. This circuit operates to shut down the inverter when the +5 volt supply exceeds 6.5 volts.

Q6 is normally biased at cutoff with 6 volts on its base and 5 volts on its emitter. An overvoltage condition results in the collector of Q6 going from 0 volts to approximately +6 volts. This drives Q5 into hard conduction and its collector places a low to NAND Gate U5-C to disable the high frequency oscillator output to the Darlington Power Drivers. This effectively shuts down the inverter assembly. The overvoltage protection circuit is not a latched circuit. If the overvoltage condition persists, the power supply will appear to turn on and off at an approximate rate of 100 Hz.

2.17.11 Power Failure Interrupt

Certain Dynamic Analyzer II operations (front panel setups) require that the volatile RAM on the Control Processor (A5A8) have continuous uninterrupted power even when the instrument is powered down. This is ensured by the use of a 2.5 volt 100 milliampere-hour nickle-cadmium battery on the Inverter assembly.

A power failure interrupt circuit (composed of U7) is employed to insure that the contents of the Control Processor Memory are not lost.

U7 monitors the primary power input via rectifier filter CR21, C54, R46. If primary power is lost, the output of U7 goes low (PFI) to the Control Processor. During normal operation the battery (BT1) will trickle charge. The battery should not be allowed to completely discharge to zero volts while connected to its normal load. Complete discharge under normal conditions would take approximately 10 days (dependent upon condition of the battery).

SECTION III

CALIBRATION

3.1 SD375 CALIBRATION PROCEDURE

3.1.1 General Information

This section contains calibration procedures for the Dynamic Analyzer II. Before attempting to perform these procedures, a good understanding of front and rear panel controls, indicators, connectors, and functional operating principles is needed. This background can be obtained by reviewing the information contained in the User Manuals (i.e., SD375, Digital I/O Interface) and all sections of the Service Instructions Manual.

The calibration procedures should *only* be performed when the results of the checkout procedure (contained in the User's Manual) indicates that calibration is necessary. Deviation from the procedures as (1) specified in the Hardware Warranty Policy and (2) as detailed in the following paragraphs is not recommended.

Upon completion of the calibration procedure, the checkout procedure should be performed to verify that the instrument meets performance requirements. Refer to the User's Manual checkout procedure.

3.1.1.1 Factory Calibration

Each unit has undergone an exhaustive calibration and functional checkout after final assembly. The instrument should rarely require calibration in the field. Calibration should *not* be attempted unless absolutely necessary and then only on those circuits which careful testing indicate adjustments are required. The checkout procedure will identify any areas requiring calibration.

3.1.1.2 Test Equipment Required

The following test equipment is required to calibrate the SD375. Alternate test and measurement equipment used to calibrate the instrument must meet or exceed the specifications of the listed equipment which follows:

Digital Voltmeter (DVM)	HP3400A	Hewlett-Packard
Oscillator	4200	Krohn-hite
RMS Voltmeter	HP3400A	Hewlett-Packard
Oscilloscope	465	Tektronix

In addition to the above, the following are required:

Shorted BNC Adapter
GR TO BNC Cable
GR (receptacle) TO BNC Adapter

WARNING

Read the following safety precautions before applying power to the equipment.

3.2 SAFETY PRECAUTIONS

3.2.1 Instrument Hazards

3.2.1.1 Explosive Hazards

The operation of the SD375 in any environment where flammable papers are present can result in an explosion. This is an unsafe practice and is therefore strongly discouraged.

3.2.1.2 X-Ray Emission/Radiation Hazards

The SD375 Display Monitor complies with the Federal Regulation for Radiation Control as required by the Radiation Control for Health and Safety Act of 1968, and as implemented by title 21, subchapter J of the Code of Federal Regulation. These regulations place certain requirements upon manufacturers of products which can emit x-rays under some conditions of operation or failure. This includes crt data display monitors.

Service technicians performing maintenance on the crt should be adequately trained in the procedures for handling (removal, installation, and use), storage, and disposal of x-ray radiation hazards. Scientific-Atlanta assumes no liability for ensuring that the provisions (as set forth in this manual) are adhered to by operator's of the crt Data Display Monitor.

3.2.1.3 Operating Hazards

The SD375 contains components which are sensitive to static electricity. The following practices should be employed whenever the printed wiring assemblies (PWAs) are removed from the instrument.

- *ALWAYS* de-energize the instrument before removing any PWAs. Whenever the procedures call for the extension of an assembly, if not stated explicitly, the removal of instrument primary power is implied.

- Avoid handling PWAs while wearing clothing that may build or hold a static charge.

- *DO NOT* allow the PWAs to rest on surfaces that may support a static charge or to be near electrically operated equipment or power lines which may induce voltages into the board.

- If PWAs are removed from the instrument for extended periods, they should be wrapped in a static conductive plastic.

3.3 SD375 Calibration Procedure

3.3.1 Preliminary Procedure

3.3.1.1 Accessing Assemblies, Test Points, and Components

In order to gain access to most of the test points and adjustments contained in the SD375, it is necessary to remove the top and/or bottom covers of the instrument. These are held in place by four (4) screws each.

The Data Display Monitor (crt) and the Power Supply Assembly covers must be removed to access crt or power supply adjustments as required. These assembly covers should normally be left in place unless repair or adjustment of the power supply or Data Display Monitor is in progress to eliminate unnecessary shock hazards and possible damage to the instrument due to the inadvertent shorting of its hardware.

When the top cover of the SD375 is removed, the Power Supply, CRT assembly, and the main card cage are exposed. Many of the adjustments on the main card cage are easily accessible without use of a card extender.

3.3.1.2 Location of Test Points and Components

Reference should be made to Figure 3-1 and the printed wiring assembly drawings of Volume II for the physical location of test/measurement points and/or adjustments throughout the instrument.

3.4 POWER SUPPLY ADJUSTMENTS

3.4.1 Preliminary Setup

Remove primary power from the SD375, remove top and bottom covers, and remove power supply assembly safety shield.

WARNING

The current capability of this power supply is sufficient to weld metals which accidentally come into contact with each other. Rings, metal watch bands and other jewelry which are worn can cause severe burns when accidental contact is made with power supply components. Remove all such objects while working on the instrument.

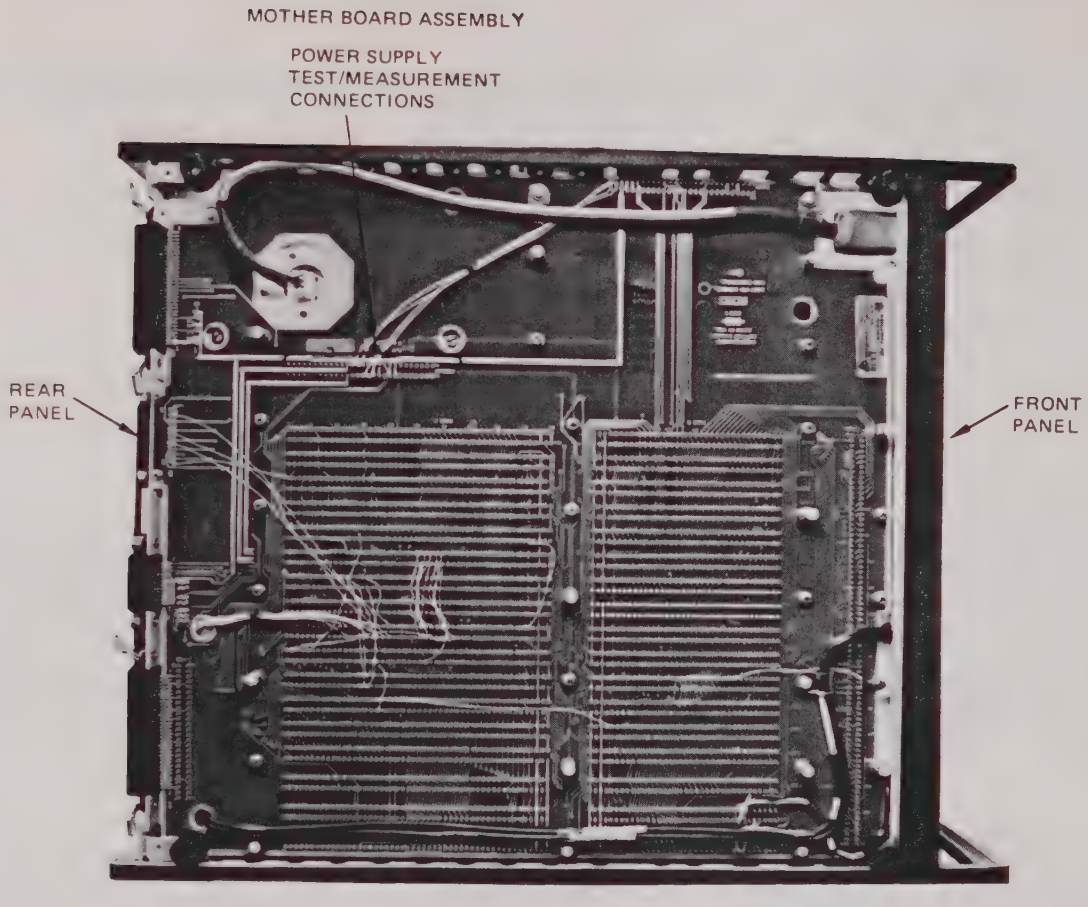


Figure 3-1. SD375 Bottom View, Cover Removed

3.4.2 Motherboard Connections

Connect the Digital Voltmeter (DVM) to ground B (low) at pins 13 and 22. These are located on the Motherboard below the power supply (under bottom cover as indicated in Figure 3-1).

3.4.3 Plus 5 Volt Connection

Connect the high to pins 1 and 12 (+5 Vdc).

3.4.4 Plus 5 Volt Measurement

Power up the instrument and check for a reading of 5.00 Vdc ±0.050V on the DVM. If the voltage is within the above limits, *no* adjustment of the 5 volt regulator is required.

If the voltage reading is low, *DO NOT* adjust the voltage until current limiting malfunctions have been eliminated as the cause of the low voltage.

3.4.5 Current Limit Visual Test

3.4.5.1 Remove power and disconnect the power cable from its' primary source. Remove the safety shield from the Power Supply Assembly (PS1).

WARNING

Lethal potentials may still be present after all AC power has been disconnected from the power supply.

3.4.5.2 Ensure that all circuit cards are properly seated in their respective slots and apply power while monitoring the LED (CR4). This LED is located on the top edge of PS1A2 (Inverter Assembly) next to the +5 volt adjustment (PS1A2R13). The printed wiring assembly drawings in Volume II will indicate the placement of this component.

The LED (CR4) should normally come on momentarily. After the +5 volt supply has settled, the LED will normally go out. If the above normal operation is observed, no adjustment of PS1A2R7 is required.

WARNING

Do not leave the power supply unattended with the safety shield removed. An unwary bystander could receive a severe shock or burn.

3.4.5.3 Power down and restore the power supply safety shield.

3.4.6 Plus (+) 5 Volt and Current Limit Adjustments

Do not attempt the following adjustments unless tests have indicated an out-of-tolerance condition and the instrument itself appears to have a power supply malfunction. If adjustment is required, turn power OFF and remove the protective cover from the power supply assembly.

3.4.6.1 Locate the Inverter Assembly (PS1A2) beneath the Power Supply safety shield. At the top edge are located the LED (CR4), the CUR LIMIT ADJ (PS1A2R7) and the +5V ADJ (PS1A2R13).

3.4.6.2 Comply with the procedures in paragraph 3.4.5.

3.4.6.3 Connect the DVM between the +5V Bus and Digital (B) Ground as in paragraph 3.4.2.

3.4.6.4 If the LED (CR4) is lit, turn the current limiting adjustment (PS1A2R7) slightly ($\approx$ 10 degrees) clockwise. If the voltage reading on the DVM does not increase, stop and troubleshoot the chassis +5 volt distribution to ensure that there are no shorts.

If no short is discovered (cause for the equipment to draw excessive current), start over at paragraph 3.4.6.4.

3.4.6.5 If the reading on the DVM is increasing, continue to turn PS1A2R7 slowly clockwise until the LED is just barely turned *off*. The voltage reading should stop increasing shortly before the LED is completely extinguished.

3.4.6.6 When the conditions in paragraphs 3.4.6.4 and 3.4.6.5 are met and the voltage read on the DVM is not within 5.000 Vdc ±0.050V, proceed to paragraph 3.4.7 (+5 volt adjustment).

3.4.7 Plus (+) 5 Volts Adjustment

Do not attempt to make this voltage adjustment to compensate for low voltage. When it has been ascertained that current limiting is not occurring as described in paragraphs 3.4.6.5, the following procedure can be performed.

3.4.7.1 Connect the DVM between pins 1 and 12 (+5 Vdc) and pins 13 and 22 (GND B) on the motherboard.

3.4.7.2 Adjust PS1A2R13 (+5V ADJ) on the Inverter Assembly for +5.000 Vdc ±0.020V.

NOTE

Once adjusted, the +5 Vdc should preferably be closer to the low end of its tolerance range.

3.4.8 Plus (+) 12 Volts Adjustment

3.4.8.1 Connect the DVM between the +12 volt bus (pins 25 and 28 on the motherboard connector) and ground C (pins 30 and 32).

3.4.8.2 On PS1A1 (Regulator Assembly) adjust R2 (+12V ADJ) for 12 volts ±0.01 volt.

3.4.9 Plus (+) 15 Volts Adjustment

3.4.9.1 Connect the DVM between the +15 volts (motherboard pin 47) and ground A (pin 35).

3.4.9.2 Adjust PS1A1R5 (+15V ADJ) for +15 Vdc ±0.01 volt.

3.4.10 Minus (−) 15 Volts Adjustment

3.4.10.1 Connect the DVM between −15 volts (motherboard pin 48) and ground A (pin 35).

3.4.10.2 Adjust PS1A1R8 (−15V ADJ) for −15 Vdc ±0.01 volt.

3.4.11 Safety Shields

3.4.11.1 Power down the instrument. Disconnect the primary power to the instrument.

3.4.11.2 If no further access to the power supply is required, remove any test connections and restore all shields, plates, and covers.

3.4.11.3 Using the Operational Checkout procedures contained in the User's Manual, ensure that proper instrument operation has been restored before attempting further calibration.

3.5 VIDEO CALIBRATION PROCEDURES

3.5.1 Data Display Monitor

If irregularities are observed in the data display monitor's presentation, the following procedures should be followed.

3.5.1.1 Review the safety precautions contained in paragraph 3.2.

3.5.1.2 Refer to Appendix A (TV50 DATA DISPLAY MONITOR) for instructions and adjustment procedures.

3.5.1.3 Adjust vertical, horizontal, focus, and centering as necessary.

3.5.2 Video Display Adjustment

3.5.2.1 With power removed from the instrument, extend the video Interface Assembly (A5A16).

3.5.2.2 Adjust the front panel GRID (G) control to the middle of its range.

3.5.2.3 Adjust the front panel Contrast (C) control to its *fully clockwise* position.

3.5.2.4 Adjust the BRIGHTNESS potentiometer (A5A19R1 located on the TV Signal Transfer board) until the horizontal raster lines on the crt just disappear.

3.5.2.5 Return the Contrast (C) control to its mid range.

3.5.2.6 Adjust the Grid (G) control so that the grid on the crt is barely visible. The DOT CURSOR should be 30 - 40% brighter than the grid.

3.5.2.7 Adjust potentiometer A5A16R26 (Y ADJ) so that the signal displayed is brighter (in intensity) than the grid lines but not as bright as the DOT CURSOR. (Refer to the Video Interface Assembly drawing in Volume II for component locations).

3.5.2.8 Adjust the VIDEO ADJ potentiometer (A5A16R27) to bring the CURSOR LINE and the annotation characters to an intensity which is slightly brighter than the grid.

3.5.2.9 Exercise the Grid (G) and Contrast (C) controls on the front panel.

3.5.2.10 Refine all adjustments by repeating the procedures in paragraph 3.5.2.2 through 3.5.2.9 until the desired contrast between the various display components (grid, signal, alphanumerics and dot cursor) is obtained.

3.5.2.11 Remove instrument power and restore the Video Interface Assembly to its slot.

3.6 INPUT SECTION ALIGNMENT

This paragraph provides alignment procedures for the Channel A and B Signal Conditioners. Signal Conditioner A is the A5A1 PWA and is identical to Signal Conditioner B (A5A2). All components referenced in the following procedure are to A5A1. These same procedures will be repeated for A5A2.

CAUTION

These procedures should be strictly followed (without deviation). If started they should be completed as they affect the overall response of the input section. Improper adjustment or failure to complete the entire procedure may result in seriously degrading the instruments performance without being readily obvious from the front panel.

3.6.1 Common Mode Rejection

3.6.1.1 Set up the oscillator (signal generator) for 52 kHz at 1 Vrms. The frequency should be verified using the frequency counter.

3.6.1.2 Select a 2 Vrms level on the SD375 front panel using the Channel A VOLTS (△▽) controls.

3.6.1.3 Connect the oscillator output through the GR TO BNC cable and a GR TO BNC adapter to the input (A or B) so that the oscillator output signal is placed on the input signal common return.

3.6.1.4 Connect the RMS voltmeter between A5A1TP1 and Test Point Ground (TP GND B) on XA1 Pins A1 and A2 of the motherboard. *Do not* extend the A5A1/A2 board.

3.6.1.5 Alternately adjust A5A1C132 and A5A1R19 for a null or minimum signal at A5A1TP1 on the RMS Voltmeter.

3.6.1.6 Repeat the adjustments of R19 and C132 (decreasing the oscillator output slightly if required) to obtain a reading of −58 dB or less on the RMS Voltmeter.

3.6.2 Input Level Compensation

3.6.2.1 Remove power from the SD375. Place the A5A1 (or A2) board on the card extender and insert it into its slot. Power up the instrument.

3.6.2.2 Remove the GR TO BNC cable and adapter and apply a normal 1 kHz signal at 48 mVrms from the oscillator to the INPUT signal BNC.

3.6.2.3 Select the 10 mV input level on the front panel.

3.6.2.4 Observe the RMS Voltmeter for a 24 Vrms reading at A5A1TP1.

3.6.2.5 Connect the RMS Voltmeter to A5A1TP2 and adjust A5A1R33 (LEVEL R MATCH) for 400 mVrms ±0.01 volt.

3.6.2.6 Connect the RMS Voltmeter to A5A1TP14.

3.6.2.7 Select the 0.01 volt input level on the front panel.

3.6.2.8 Adjust the oscillator output for 1 kHz and a reading of −2 dB on the RMS Voltmeter. The oscillator output should be approximately 600 mVrms with the RMS meter on the −10 dB level.

3.6.2.9 Adjust the oscillator frequency for 100 kHz and adjust C31 to read −2 dB ±0.1 dB.

3.6.2.10 Select the 0.02 Vrms input level using the front panel VOLTS $\Delta\nabla$ controls.

3.6.2.11 Adjust the oscillator output for 1 kHz and a reading of −2 dB at A5A1TP14.

3.6.2.12 Adjust the oscillator to 100 kHz.

3.6.2.13 Adjust A5A1C29 to return the reading on the RMS Voltmeter to −2 dB at A5A1TP14.

3.6.2.14 Select an input level of 0.05 Vrms on the SD375 front panel.

3.6.2.15 Adjust the oscillator to provide a 1 kHz signal and a reading of −2 dB at A5A1TP14.

3.6.2.16 Adjust the oscillator frequency to 100 kHz.

3.6.2.17 Adjust A5A1C28 to return the reading on the RMS Voltmeter (at A5A1TP14) to −2 dB.

3.6.2.18 Repeat the procedures in paragraphs 3.6.2.3 through 3.6.2.17 until no further adjustment is necessary to achieve the above readings.

3.6.3 Preamplifier DC Offset Adjustment

3.6.3.1 Disconnect the oscillator and short the input with a shorted BNC adapter.

3.6.3.2 Select the 10 mVrms INPUT LEVEL and DC coupling on the SD375 front panel.

3.6.3.3 Adjust A5A1R34 (OFFSET) for 0.000 Vdc ±0.010V at A5A1TP14.

3.6.3.4 Select the 1 volt INPUT LEVEL on the SD375 front panel and observe the RMS Voltmeter reading at A5A1TP14 (0.000 Vdc ± 0.050V).

3.6.3.5 Record the reading.

3.6.3.6 Select the 10 mV INPUT LEVEL.

3.6.3.7 Adjust A5A1R34 for the same reading at A5A1TP14 recorded in paragraph 3.6.3.5 ±0.005 volts.

3.6.3.8 Repeat the procedures contained in paragraphs 3.6.3.2 through 3.6.3.7 until the offset reads 0.000 Vdc ± 0.010 volts for both input levels.

3.6.3.9 Remove primary power to the instrument and restore the Signal Conditioner to its slot.

3.6.3.10 Repeat the Preamplifier DC Offset adjustments for the A5A2 board if required.

WARNING

NO ATTEMPT SHOULD BE MADE BY FIELD PERSONNEL or REPRESENTATIVES OF THE CUSTOMER TO ALIGN THE ELLIPTICAL FILTERS (LOW PASS FILTERS) CONTAINED ON SIGNAL CONDITIONERS A or B (A5A1 or A5A2 assemblies).

These circuits were calibrated to provide specific bandpass characteristics at the factory and should not require adjustment in other than extreme conditions. Should the elliptical filter assemblies require extensive repair, and their performance characteristics become suspect, the customer should request the services of the Customer Service Department of Scientific-Atlanta to effect the repair and/or alignment of those assemblies.

ANY ATTEMPT BY FIELD PERSONNEL TO ALIGN THE ELLIPTICAL FILTERS CAN RESULT IN SERIOUSLY DEGRADING THE PERFORMANCE CHARACTERISTICS OF THE INSTRUMENT.

3.7 NOISE FLOOR, LINEARITY AND A/D ADJUSTMENTS

3.7.1 Noise Floor Baseline Adjustments

3.7.1.1 Select the SINE DITHER *OUT* position of A5A6S1.

3.7.1.2 Extend the Signal Conditioner, power-up, and press the PANEL, 0, and RCL touch controls. Connect a shorted BNC adapter to the input.

3.7.1.3 On the front panel of the SD375, select 10 kHz RANGE, 1V input LEVEL, +20 dB GAIN, EXPOnential averaging, and 16 averages.

3.7.1.4 Adjust A5A1R181 for a baseline between −80 dB and −82 dB on the Data Display Monitor. If any spurs extend above the −60 dB grid line, the Common Mode Rejection or other adjustments may need to be refined depending on the frequency of the spurs. This problem may be caused by noise induced in the extended A5A1 board or marginal components of the input or A/D Converter generating noise.

3.7.2 Sine Dither

3.7.2.1 Place the SINE DITHER switch (A5A6S1) in the *IN* position.

3.7.2.2 Connect the oscilloscope at A5A1TP16.

3.7.2.3 Adjust A5A1R53 for 100 mV peak-peak ±20 mV

3.7.2.4 Power down and restore A5A1 to its slot. Extend A5A3 and connect the oscilloscope probe to A5A3TP1.

3.7.2.5 Power up and depress the PANEL, O, and RCL touch controls. Adjust A5A3R106 for 100 mV peak-peak ±20 mV at A5A3TP1.

3.7.2.6 Adjust A5A3R107 for 100 mV at A5A1TP9.

3.7.2.7 Check both channels (A and B) to ensure that there is no power supply 26 kHz and 52 kHz components present on the Data Display Monitor. If there is a ripple component, proceed with paragraph 3.7.2.8.

3.7.2.8 Select an INPUT LEVEL of 100 mV for both Channels A and B. Select 100 khz range and apply an input signal of 12 kHz ± 0.5 kHz and an amplitude of less than 10 mVrms. Any ripple component present should not appear above the −55 dB level on the Data Display Monitor. Readjust A5A3R106 (Channel A) and A5A3R107 (Channel B) until any ripple disappears.

3.7.3 A/D Converter Adjustments

3.7.3.1 Place the SINE DITHER switch on the A5A6 assembly in the *OUT* position.

3.7.3.2 Short the *INPUT* signal BNC with the shorted BNC adapter.

3.7.3.3 Extend the A5A1/A2 assembly.

3.7.3.4 Power up and depress the PANEL, O, RCL touch controls. Depress the AC coupling touch control and ensure that DC coupling is selected.

3.7.3.5 Adjust A5A1/A2R175 (A/D OFFSET) for a 0.00 Vdc ± 0.001V (1 mV) reading on the DVM at A5A1/A2TP13. Move DVM to TP18 and adjust R8 for 0.00 Vdc ±0.001V (1mV).

3.7.3.6 Select TIME mode on the SD375 front panel and adjust A5A1/A2R9 if the display is not centered.

3.7.3.7 Apply a 4.0 kHz ± 500 Hz signal at 1.0 Vrms ± 0.05V to the input signal BNC.

3.7.3.8 Select LOG Y on the front panel. The grid Y parameters should be expressed in dB on the Data Display Monitor.

3.7.3.9 Move the CURSOR to the top of the 4 kHz signal and ensure that the displayed signal is symmetrical.

NOTE

CURSOR readout of nonsymmetrical signals will result in out of tolerance or invalid RMS or dB values. If the signal is nonsymmetrical adjust the output frequency of the oscillator for symmetry.

3.7.3.10 Adjust A5A1/A2R188 for a 00.00 dB reading on the Data Display Monitor.

3.7.3.11 Return the Sine Dither switch (A5A6S1) to its *IN* position.

3.7.4 Linearity Checks and Adjustments

3.7.4.1 Apply 12 kHz ± 500 Hz at 1.000 Vrms ± 0.005V from the oscillator to the input BNC connector (Channel A or B).

3.7.4.2 Depress the PANEL, O, and RCL touch controls. Select the appropriate 1 volt input LEVEL and the 20 kHz range on the front panel. Move the CURSOR to the top of the 12 kHz signal on the Data Display Monitor.

3.7.4.3 Adjust the Sine Dither A5A1/A2R53 for the best overall linearity between the −50 dB and −60 dB points on the display using the front panel gain settings and Y-axis readings listed in the following table.

Table 3-1. Linearity Readings

Input	Y-Reading
0 dB	0 ± 0.2 dB
−10 dB	−10 ± 0.3 dB
−20 dB	−20 ± 0.3 dB
−30 dB	−30 ± 0.4 dB
−40 dB	−40 ± 0.5 dB

Table 3-1. Linearity Readings (Continued)

Input	Y-Reading
−50 dB	−50 ± 1.0 dB
−60 dB	−60 ± 1.5 dB
−62 dB	−62 ± 1.5 dB
−64 dB	−64 ± 1.5 dB
−66 dB	−66 ± 2.0 dB
−68 dB	−68 ± 2.0 dB
−70 dB	−70 ± 2.0 dB

3.7.4.4 If any of the specifications in Table 3-1 are not met, refine the adjustments in paragraphs 3.7.1 through 3.7.4.

3.7.4.5 Restore the A5A1/A2 assembly.

3.8 TEST/CAL CIRCUIT ADJUSTMENTS

3.8.1 Clock Frequency Adjustments

3.8.1.1 Extend the Timing and Control Assembly (A5A6).

3.8.1.2 Power-up and depress the PANEL, O, RCL touch controls.

3.8.1.3 Connect the frequency counter to U17 pin 3.

3.8.1.4 Adjust A5A6C12 for a frequency reading of 1.024 MHz ± 3 Hz.

3.8.2 TEST/CAL Adjustment

3.8.2.1 Press the TEST touch control.

3.8.2.2 Move the CURSOR to the top of the CAL signal.

3.8.2.3 Adjust A5A6R13 (CAL SIG) for a reading of −10.0 dB on the Data Display Monitor.

3.9 ANALOG PLOTTER OUTPUT ADJUSTMENTS

3.9.1 Extend the A5A3 assembly.

3.9.2 Power-up and select the PANEL, O, and RCL touch controls.

3.9.3 Adjust A5A3R91 (10V ADJ) for a reading of +10 Vdc ± 0.001 volts at A5A3TP17 (10V REF) on the DVM.

3.9.4 Connect the DVM to the PLOTTER X output on the rear panel of the SD375.

3.9.5 Alternately select *TIME* and *SPECT* functions on the front panel while in the *CAL*, *FS* mode and adjust A5A3R97 for the same reading (+10 Vdc ± 0.001V) on the DVM.

3.9.6 Power-down and restore the A5A3 assembly to its slot.

3.10 CHECKOUT PROCEDURE

Operational checkout procedures are contained in the Operator's Manual (part number 21941600) Section IV. These procedures should be performed after calibration to verify that the instrument meets performance requirements.

SECTION IV

MAINTENANCE AND PARTS INFORMATION

4.1 MAINTENANCE

4.1.1 Maintenance Philosophy

4.1.1.1 Operator Maintenance

Maintenance, as performed by an operator of the Dynamic Analyzer II, is limited to (1) operational checkout procedures, (2) performance of the SD375 Self Test, (3) cleaning of external instrument surfaces, and (4) the performance of the operator checks (inspections) specified in the Operator's Manual. These procedures are detailed in Section IV of the Operator's Manual (part number 21941600) and specifically paragraphs 4-1 through 4-54.

4.1.1.2 Servicing

Servicing is defined as that *maintenance*, performed by a service engineer or technician, which includes (1) the troubleshooting of the instrument, its major (or minor) assemblies and components, (2) the replacement of defective assemblies or component hardware, and (3) the alignment and calibration of the Dynamic Analyzer II in accordance with procedures contained in this manual. Maintenance personnel (i.e., service engineers, service technicians, electronics technicians) may also be required to perform the procedures specified in paragraph 4.1.1.1 above.

The information which follows is specifically included in the manual as an aid to the service engineer or technician with knowledge of and experience in the maintenance (repair) of *processor-based* digital and analog systems.

4.1.2 Servicing and Repair Procedures

The information provided to assist the service engineer (in the diagnosis of problems within the SD375 Dynamic Analyzer II) is not limited to the use of documentation supplied as part of the SD375 Dynamic Analyzer II Service Instructions. This information must be utilized in conjunction with the skills exemplified by personnel who are qualified as described in the preceding paragraph.

4.1.2.1 Information Supplied

The following information is summarized to facilitate locating needed service information:

- Operational checkout procedures are contained in Section IV of the Dynamic Analyzer II Operator's Manual which is provided with each instrument. These procedures should be employed prior to those contained in this manual.

- Detailed Circuit Analyses of all major assemblies with functional block diagrams are contained in Section II, V and Appendix A of this manual. These sections should be read and understood before attempting to service the instrument.

- Detailed schematics and printed wiring assembly drawings are contained in Volume II of this manual. These diagrams and drawings provide hardware pin readout information and test point or component location. In many cases, test points identified are accompanied by descriptive signal parameters and/or voltages.

- The Wire String List is contained in Appendix B. This document (when used in conjunction with the detailed schematics of Volume II) is an invaluable aid when circuit tracing. The source and destination of all signal callouts for each major assembly within the SD375 is provided.

- Self Test and I/O Interface Diagnostics can be useful in isolating problems and are described in the paragraphs which follow.

- Parts information is contained on the detailed schematic diagrams of Volume II as well as in Section 4.2 where part numbers of major assemblies, special integrated circuits, controls, and indicators are identified.

- Calibration procedures are contained in Section III of this manual.

- Additional assistance in the diagnosis of problems may be obtained from the Scientific-Atlanta Spectal Dynamics Division Customer Service Department.

4.1.3 Self Test

The Self Test which has been incorporated in the SD375 allows the operator to exercise most of the hardware (approximately 95 percent) using an internally generated test signal. This signal resides at cell 256 with an amplitude of -10 decibels from full scale. Its amplitude and cell location are constant. The self test, if used properly, can provide clues to problem areas when the instrument malfunctions.

4.1.3.1 Performing the Self Test

The Self Test is initiated by pressing the following touch controls in the indicated sequence.

PARAMETERS Group

Press PRGM
Press 5

FUNCTION Group

Press LIST

The menu will appear on the data display monitor as follows:

```
SELF TEST

* 1.  OFF
  2.  ON
```

The Self Test program is then activated using one of the following methods:

Method 1

FUNCTION Group

Using the SEL UP/DOWN (△, ▽) touch controls, press DOWN(▽). The asterisk on the menu will move to selection 2 (ON).

Press OPER. This activates the Self Test.

Method 2

PARAMETERS Group

Press 2
Press ENT (the asterisk will move to selection 2 (ON))

FUNCTION Group

Press OPER. This activates the Self Test.

The entire test sequence will be implemented for Channel A and then Channel B. When both test sequences are completed, test results will be displayed on the crt as described below.

```
SELF TEST

CH A        CH B

1. F        1. F
2. F        2. F
3. F        3. F
4. F        4. F
5. P        5. P
6. F        6. F
7. P        7. P
8. P        8. P
```

The Self Test results for each channel are indicated by either a "P" for pass or an "F" for fail as shown in the list. There are seven tests for each channel. Test eight (8) indicates a Time-Out failure.

A Time-Out failure will occur if the entire test sequence for both channels (A and B) is not completed within 20 seconds. The time normally required to complete the self test is 20 seconds; 10 seconds per channel. If all tests for a single channel are not completed within 20 seconds, the remaining tests (which have not been performed) will result in "F" being displayed (including Test 8).

The Self Test results displayed on the crt will remain on the display until any front panel touch control is pressed. If the Self Test results in all "P's", the results will remain displayed on the crt for 20 seconds. The front panel setup which was present before the Self Test was initiated will then be restored.

The configuration of the front panel when the Self Test is initiated is described as follows:

Hz
dB
AC
YLOG
SPECT
LIN AVG
MAX
XLIN
HANN
YGAIN = 0 dB
TRANSLATOR GAIN = 0 dB
TRANSLATOR ZOOM = 10
AVG N COUNT = 10
INPUT LEVEL = 1V
ANALYSIS RANGE = 10 kHz

4.1.3.2 Interpreting Self Test Results

The table which follows (Table 4-1, Self Test Matrix) depicts the hardware that is exercised when the Self Test is initiated. Information displayed includes test numbers (1–7), test functions, and the percentage of hardware on affected assemblies that is exercised to perform the test function.

The percentage of hardware not exercised is tabulated at the bottom of the table and is depicted in Figure 4-1 (Self Test Functional Block Diagram).

4.1.3.3 Hardware Not Tested

Of the three major assemblies which are not tested in entirety (A5A3, A5A9, A5A17), two are optional (A5A9 and A5A17) and may or may not be installed on the instrument. I/O Interface Assembly (A5A9) diagnostics are contained in paragraphs which follow.

Table 4-1. Self Test Matrix

TEST NUMBER	TEST FUNCTION	PRINTED WIRING ASSEMBLY HARDWARE EXERCISED (%)																	
		SIGNAL CONDITIONER A5A1	SIGNAL CONDITIONER A5A2	100 kHz LPF/PLOTTER A5A3	TRANSLATOR A5A4	TRANSLATOR FILTER A5A5	TIMING & CONTROL A5A6	INPUT MEMORY A5A7	CONTROL PROCESSOR A5A8	I/O INTERFACE A5A9	MULTIPLIER A5A10	μPROGRAM CONTROL A5A11	ARITHMETIC PROCESSOR A5A12	PROCESSOR MEMORY A5A13	CURSOR CONTROL A5A14	MEMORY ADDRESS A5A15	VIDEO INTERFACE A5A16	SSG A5A17	FRONT PANEL INTERFACE A5A18
1	REAL TIME SPECTRUM	80	80				61	90	100		100	100	95	60	80	100	100		95
2	M1 AVERAGE												5	20					
3	TRANSFER TO M2													20					
4	PLUS 1 AVERAGING								*				5	20					
5	M1 ERASE								*				5	20					
6	VOLTS /EU/ PSD								#			#							
7	TRANSLATOR				99	100													
	HARDWARE NOT EXERCISED	20	20		1		39	10							20				5

HARDWARE NOT EXERCISED

* EXERCISES NEW AREA OF Z80 PROGRAM

\# EXERCISES NEW AREA OF SIGNAL PROCESSING PROGRAM

The 100 kHz Low Pass Filter and Plotter Assembly (A5A3) and the Synchronous Signal Generator (A5A17) may be tested using externally applied excitation or sources in conjunction with appropriate front panel touch controls as necessary and appropriate measurement or display devices (oscilloscope or plotter) to determine circuit integrity.

This approach to diagnosing problems associated with all of the *hardware not exercised* (from Table 4-1) will be similar.

The particular circuits not tested are:

A5A1 — Input Coupling, Common Mode Rejection, Variable Gain Amplifier, and the Low Pass Filter I - IV

A5A2 — Same as A5A1

A5A3 — 100 kHz Low Pass Filter and Plotter circuitry

A5A4 — Translator overload indicator circuitry

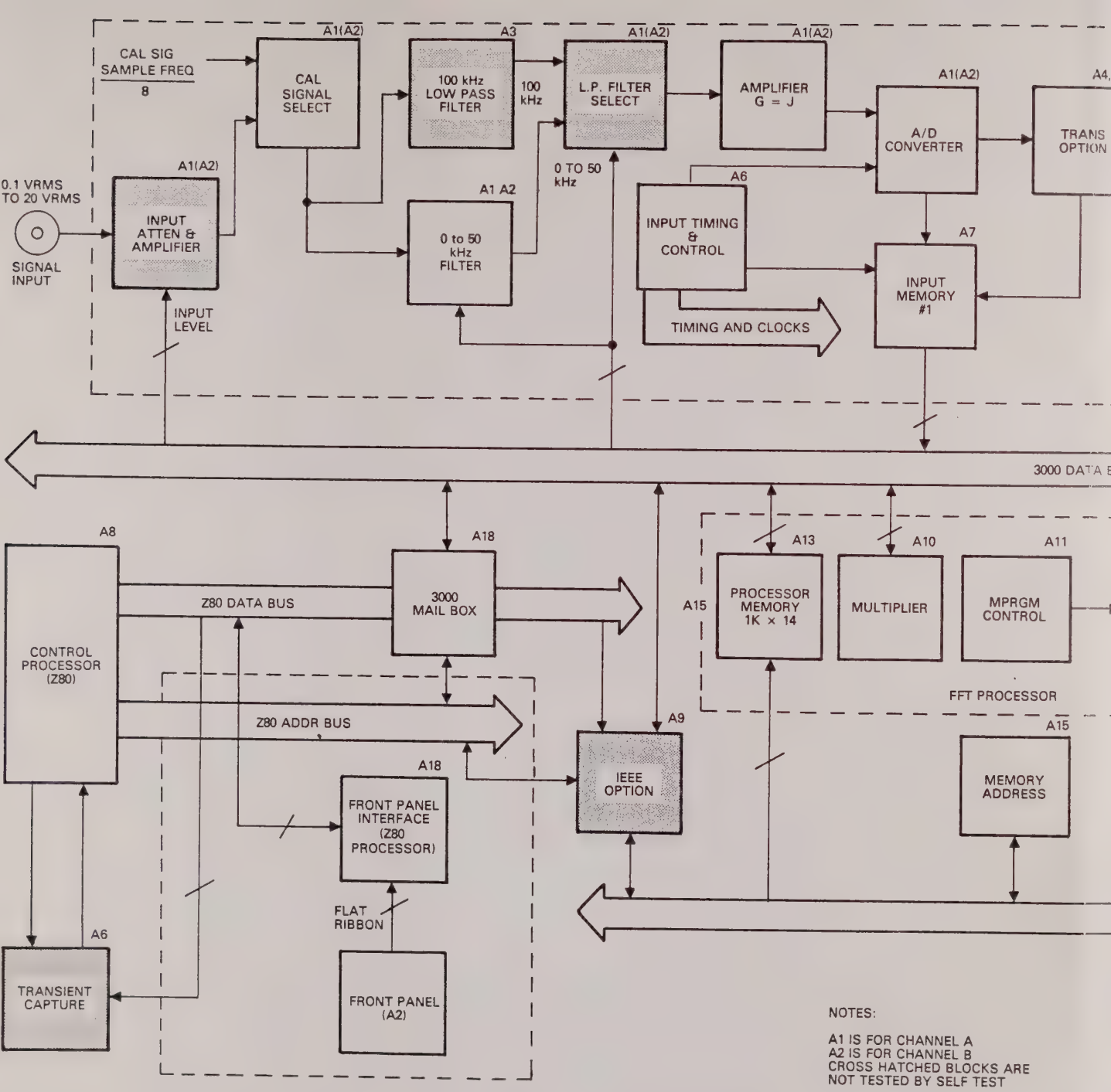
A5A6 — Memory Hold and Transient Capture circuitry

A5A7 — Zero and Rotate circuitry

A5A9 — The entire assembly is not tested. Refer to procedures contained in the following paragraph.

A5A14 — Harmonic mode, display mode, and line cursor circuitry is not exercised.

A5A18 — External averaging and transient capture switches are not tested.



NOTES:

A1 IS FOR CHANNEL A
A2 IS FOR CHANNEL B
CROSS HATCHED BLOCKS ARE NOT TESTED BY SELF TEST

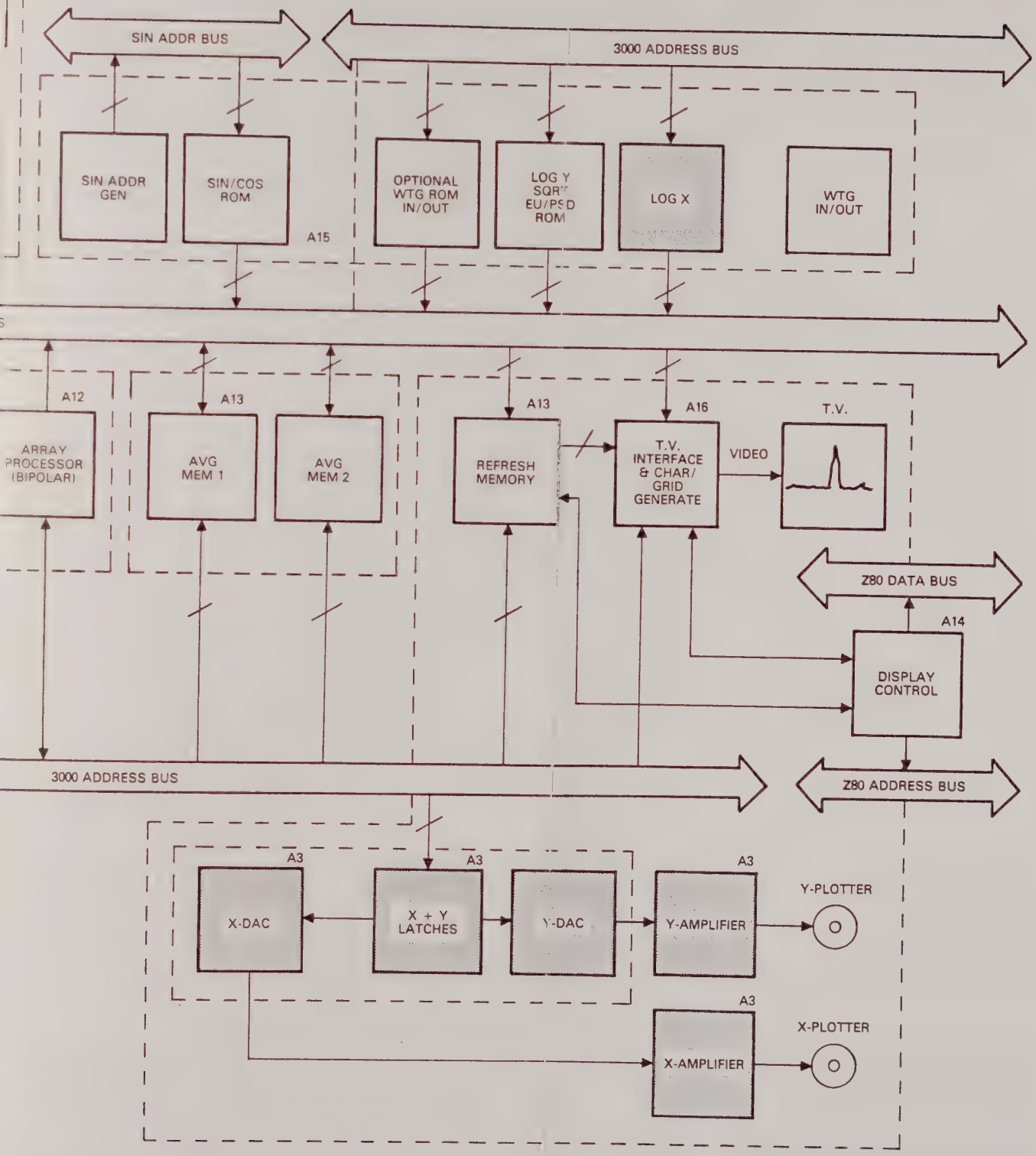


Figure 4-1. SD375 Self Test Functional Block Diagram

4.1.4 I/O Interface Assembly Diagnostics

The procedures contained in the following paragraphs should provide a logical approach to the diagnosis of I/O Interface Assembly malfunctions. These procedures have been summarized in Figure 4-2 and are amplified in the paragraphs which follow.

4.1.4.1 Preliminary Procedures

The following procedures should be performed to restore normal operation before implementing the Troubleshooter's Diagnostic Routine. Verify that:

- Proper operating procedures are employed in accordance with the Digital I/O Interface Instruction Manual (part number 21803300).
- All rear-panel and other external interconnecting cables are properly mated.
- The I/O Interface Assembly (A5A9) and all other printed wiring assemblies are properly seated in the chassis.
- The Self Test has been performed to eliminate the possibility of other malfunctions within the SD375.

4.1.5 Diagnostic Routine

When the preliminary measures of resolving I/O Interface Assembly malfunctions have been performed and a problem still exists, perform the diagnostic routine in accordance with Figure 4-2 and the following:

4.1.5.1 Observe the power-up cycle of the I/O (A5A9) for normal operation. This is accomplished by applying power to the instrument and monitoring the on-card LED display.

NOTE

The LEDs on the A5A9 PWA can provide clues to a possible problem with the assembly.

When the SD375-3xxx is initially "powered-up" the I/O Card Status LEDs assume the configuration described in Figure 4-3. These LEDs are physically layed out as indicated. On power-up, one of the two status configurations indicated is assumed based on the operating mode.

If a normal "power-up" was observed, look for problems in the GPIB (IEEE 488) and/or ACE (RS-232-C) output lines, drivers, I/O card connector pins associated with data input or output, and signal lines to/from J20 and/or J21 on the rear panel.

If a normal "power-up" was *not* observed, perform the steps in paragraph 4.1.5.2.

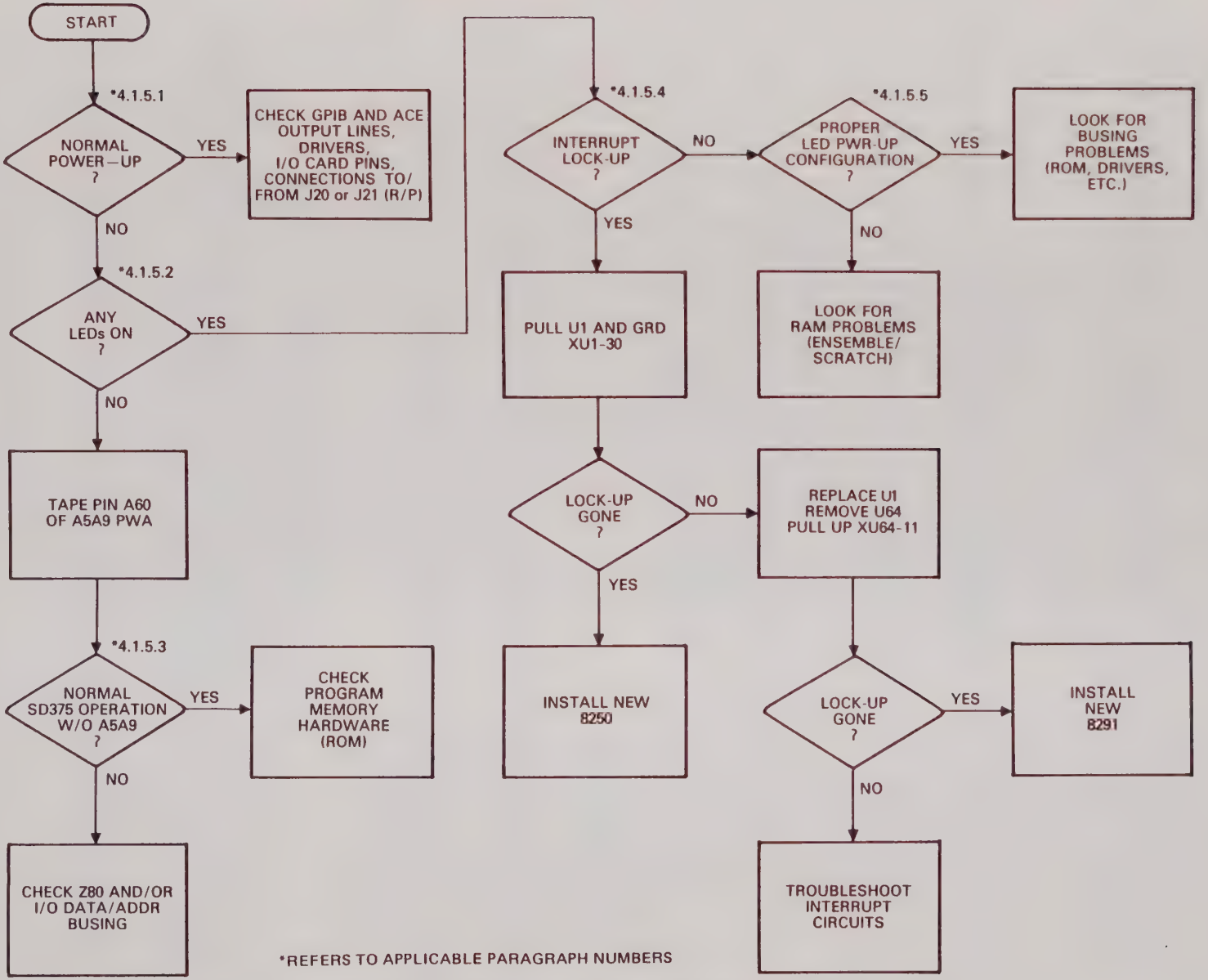


Figure 4-2. I/O Interface Assembly (A5A9) Troubleshooter's Diagnostic Routine

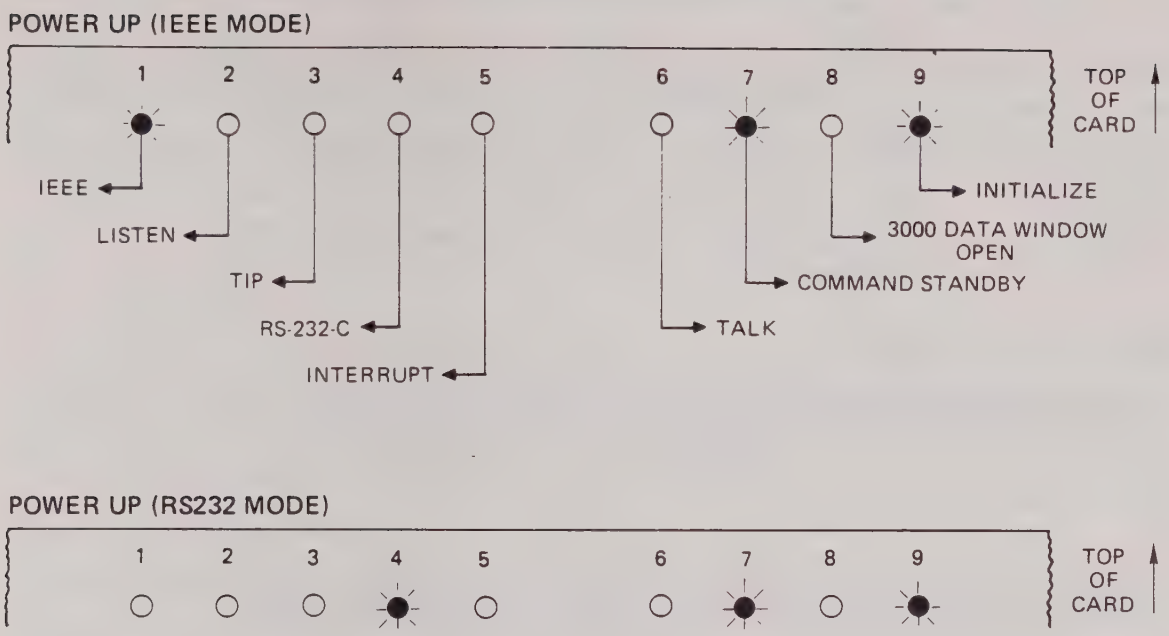


Figure 4-3. I/O Interface Status LEDs (Power-Up Configuration)

4.1.5.2 Are Any LEDs On

Observe the status LEDs. If no LEDs are lit, remove the power from the instrument. Remove the I/O card and place a strip of cellophane tape over pin A60. Insert the I/O card into its slot and ensure that it is properly seated. Power up the SD375. Perform the procedures contained in paragraph 4.1.5.3.

CAUTION

This procedure is employed to detect possible ROM problems. The technician should use only very thin tape to avoid damage to the Motherboard receptacle A1A1-XA9. The TAPE MUST BE COMPLETELY REMOVED (when the test is completed) to ensure proper mating of connector pins when the assembly is reinstalled.

If a normal "power-up" was experienced, and there were LEDs lit, perform the steps detailed in paragraph 4.1.5.4.

4.1.5.3 SD375 Normal Operation

With pin A60 taped (open circuited), check to see if the SD375 operates normally. The taped pin (A60) essentially takes the I/O card out of the SD375 by telling the control processor that the -3xxx option is not installed. If normal operation results, check the I/O Card Program Memory (ROM), its associated logic, and hardware.

If (when A5A9 pin A60 is taped) normal operation does *not* result, check for contention on the Z80 and/or I/O card data and address buses.

4.1.5.4 Interrupt Lock-Up

An Interrupt Lock-Up is indicated by LED number (5) coming *on* and remaining *on* at all times. This could result from the GPIB chip (8291) not having received a message to invert the interrupt logic. If the light turned off, it will be due to the attempt (by software) to reinitialize the I/O card, and (in most cases) would be imperceptible.

If a "lock-up" is observed, power down the instrument, remove the A9 card, remove U1, and install a ground clip at pin 30 of XU1. Insert the I/O card and power up the instrument.

If the "lock-up" *does not* occur, the ACE chip (RS-232-C) U1 is defective and must be replaced.

If the "lock-up" *does* occur, power-down the instrument, remove the I/O card, remove the ground at pin XU1-30, and restore U1 to its pocket. Remove U64. Install a +5 volt pullup to pin 11 of XU64 through a 4700 ohm resistor. Insert the I/O card in its slot ensuring that it is properly seated and power-up the instrument.

If the "lock-up" *does not* occur, the GPIB chip (U64) is defective.

If the "lock-up" does occur, there are other problems within the interrupt circuitry which will require troubleshooting.

If no interrupt lock-up exists, perform the procedures in paragraph 4.1.5.5.

4.1.5.5 Proper LED Power-Up Configuration

If the I/O card problem has not been isolated, verify that a proper power-up configuration of the I/O Card Status LEDs is observed.

If not observed, look for problems with the Ensemble Data RAM, the Scratch Pad RAM, or their associated logic and hardware.

If a proper power-up LED configuration is displayed, look for bus contention. Busing problems could have occurred on the PROMs, their drivers, or associated logic and hardware.

4.1.6 I/O Interface Assembly Status LED Configuration Summary

The I/O Status LEDs will assume various on/off configurations during normal operation. Figure 4-4 summarizes these configurations. Status LED functions are also defined.

By monitoring the I/O Card Status LEDs, the technician can sometimes gain information which will lead to defining problem areas. This process was employed in the troubleshooter's diagnostic routine (detailed in the preceding paragraph).

4.1.6.1 RAM Failures

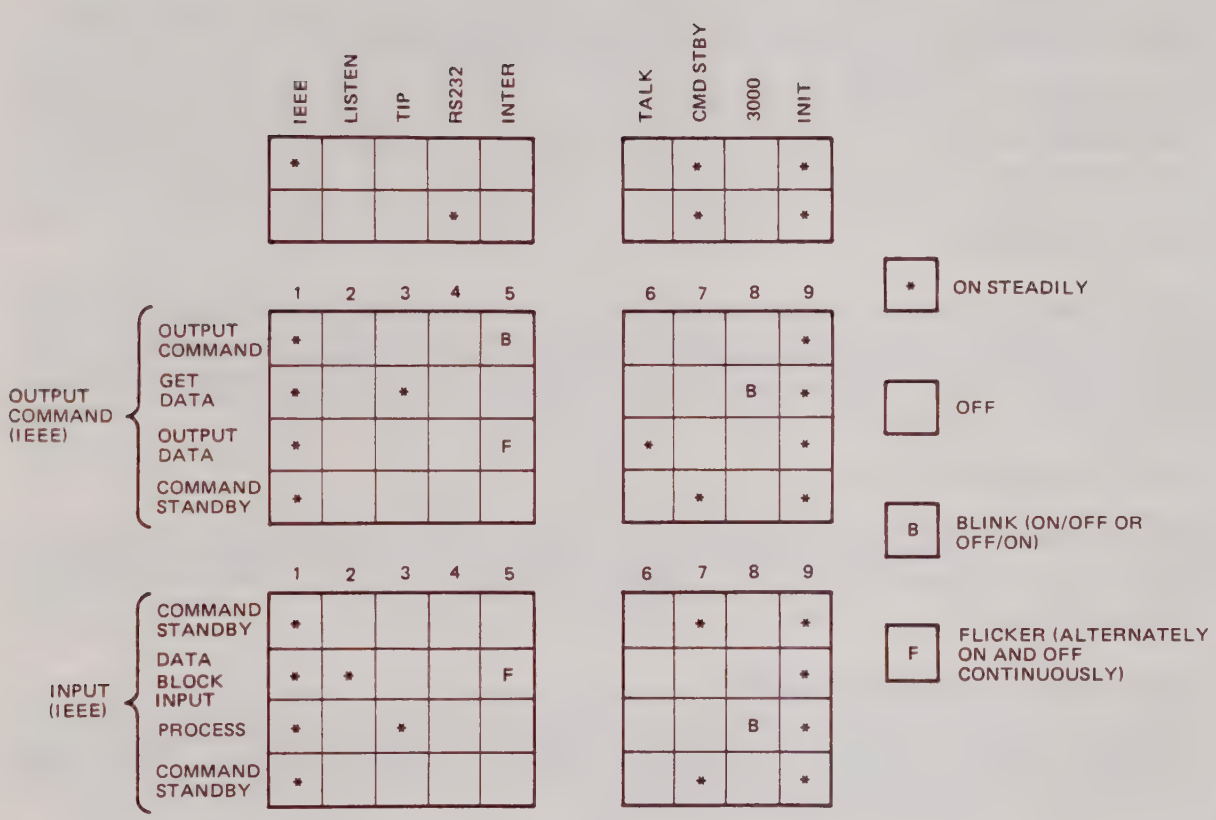
One of the key indicators that there may be a malfunction in the I/O Card RAM (Ensemble Data RAM or Scratch Pad RAM) is erroneous LED configuration after power-up initialization is completed. An incorrect pattern would be indicated by LEDs coming *on* that should be *off* and LEDs going *off* that should be *on*.

4.1.6.2 INTERRUPT (LED 5)

The INTERRUPT LED will normally flicker (on and off) at varied rates (dependent upon the number of data blocks being transferred) or appear to remain on but its glow will not be as brilliant as if it were on constantly.

4.1.6.3 3000 Data Window Open (LED 8)

In normal operation, when 3000 data is being read or written, the 3000 LED will come *on* briefly while the transfer is in progress. Because the transfer occurs very rapidly, the 3000 LED is lit for a very short period (sometimes a flicker that is barely perceptible).



1. IEEE	Indicates that the IEEE port is active.
2. LISTEN	Indicates that the I/O is actively inputting data.
3. TIP	"Task In Progress" — this LED indicates that I/O is processing data (preparing it for output, or responding to an input block.
4. RS-232-C	Indicates that the RS-232-C port is active.
5. INTERRUPT	I/O responses to "outside world" activities are interrupt driven — this LED flashes as I/O reacts to the outside world's stimuli.
6. TALK	Indicates the I/O is actively outputting data.
7. Command Standby	The I/O is quiescent, waiting for task directions.
8. 3000 Window	The I/O memory is opened to the 3000 for data read or write.
9. Initialize	I/O is initialized, ready to be operated. This LED is turned off when LOGO RESET is depressed.

Figure 4-4. I/O Interface Assembly Status LED Configurations Summary

4.2 REPLACEMENT PARTS

This section contains the parts lists for all major assemblies of the SD375 Dynamic Analyzer II, the special (configuration-controlled) parts which must be ordered from the factory, and a list of common controls and indicators used in the SD375.

Instructions for procuring common hardware and special parts are provided along with sources of hardware descriptive information not contained in these pages.

4.2.1 Where to Find Parts Information

Most of the hardware used in the SD375 is common electronic hardware (i.e., resistors, capacitors and integrated circuits) that are identified (by component reference designator, vendor or Scientific-Atlanta part number, and tolerances) in the detailed schematic diagrams of Volume II. Reference to vendor specifications or data sheets and/or cross reference lists should be made if more detailed information is required.

Tables 4-2 through 4-4 list part numbers of all major assemblies, the special (configuration-controlled) integrated circuits (ICs) used, and controls and indicators of the SD375. All parts listed in Tables 4-2 and 4-3 must be procured from Scientific-Atlanta. The controls and indicators listed in Table 4-4 are (for most parts) common hardware. They are included here in a quick reference listing to facilitate replacement.

4.2.2 Obtaining Standard Hardware

Standard or common hardware may be procured through any local distributor of standard electronic hardware. However, Scientific-Atlanta maintains a complete stock of all parts (assemblies and components) used in the instrument.

4.2.3 Ordering Parts From the Factory

When requisitioning parts from Scientific-Atlanta, the following information should accompany each order.

- Part Reference Designator (i.e., A1, A5A7, A5A1U65)
- Part Number — Indicate the Scientific-Atlanta 8-digit part number (if available)
- Description — (i.e., PROM set, INP 11, 12, 13, 14, 15)
- Assembly Number — (i.e., A3, CRT Assembly; A5A9, I/O Interface Assembly)
- Serial Number — Indicate the serial number of the instrument (found on rear panel ID plate)
- Model Number — Indicate the full model number with any option designators (dash numbers) of your instrument (i.e., SD375-1; SD375-3B01; SD375-2).
- Revision Letter — Indicate any revision letter inscribed on the major assembly containing the part being ordered. The revision letter will appear as indicated in the following samples: REV B or REVISION E.

Table 4-2. Special Replaceable Parts List (Major Assemblies)

Assembly No.	Part No.	Description
A1	21050400	Main Frame Assy
A1A1	21851500	Motherboard
A1A2	21237800	Chassis Assy
A2	21861300	Front Panel Assy
A2A1	21243000	Input Interface Assy
A3	21054500	CRT Assy
A4	21214700	Rear Panel Assy
A4A1	21211400	BNC Interface Assy
A5	21053600	Printed Wiring Assy Set
A5A1	21848300	Signal Conditioner A
A5A2	21848300	Signal Conditioner B
A5A3	21232700	100 kHz Low Pass Filter & Plotter
A5A4	21180600	Translator (-1 Option)
A5A5	21284500	Translator Filter Output (-1 Option)
A5A6	21837200	Timing and Control Assy
A5A7	21046700	Input Memory Assy
A5A8	21850200	Control Processor Assy
A5A9	21255300	I/O Interface Assy (-3 Option)
A5A10	21040700	Multiplier Assy
A5A11	21846300	Microprogram Control Assy
A5A12	10496500	Arithmetic Processor Assy
A5A13	10496800	Processor Memory Assy
A5A14	21084000	Cursor Control Assy
A5A15	21013300	Memory Address Assy
A5A16	21860300	Video Interface Assy
A5A17	21876500	Synchronous Signal Generator (-4 Option)
A5A18	21149900	Front Panel Interface Assy
A5A19	21081500	TV Signal Transfer Assy
PS1	21025102	Power Supply Assy
PS1A1	21025300	Regulator Assy
PS1A2	21025500	Inverter Assy
PS1A3	21047003	Power Panel Assy

Table 4-3. Special Replaceable Parts List (Integrated Circuits)

Assembly No.	Reference Designation	Part No.	Description
A5A1/A2	U65	21848600	PROM (Analysis Range)
	U53	21135900	PROM (Level)
A5A4	U35, 48, 51, 57	21367300	PROM SET (XSN24, XSN13, TLR2, TLR1)
A5A5		21367400	PROM SET (XCF13, XCF24, TLR3-6, PRE1, 2)
	U11	21318704	Programmable Logic Array (XOF)
	U37	21138703	Programmable Logic Array (XSL)
	U55	21138701	Programmable Logic Array (XSM)
A5A7	U3-6, U16	21254400	PROM SET (INP 11, 12, 13, 14, 15)
A5A8	U5-10	21850700	PROM SET, Z80 MCI-1 through -6
A5A9	U70-73	21260700	PROM SET (PROM 1, 2, 3, 4)
		21260902	PROM SET (3B02 Option)
		21260900	PROM SET (3B00 Option)
		21260901	PROM SET (3B01 Option)
A5A11		21846400	PROM SET
	U1-8, 15-22, 30-37, 71-73	21240500	PROM SET
A5A14	U43	21103200	PROM (TVXFR)
	U14, 15	21392100	PROM SET (CURS 1, CURS 2)
A5A15	U42, 56	21246400	PROM SET (COS ROM, COS LSBs)
	U41, 55	21246500	PROM SET (SIN ROM, SIN LSBs)
	U40, 54	21246600	PROM SET (SQRT/LOG Y ROM & LSBs)
	U39, 53	21246700	PROM SET (DIVIDE/TAN ROM and LSBs)
	U38, 52	21246800	PROM SET (LOG X ROM, LOG X LSBs)
	U37, 51	21246900	PROM SET (WEIGHT ROM and LSBs)
	U36, 50	21247000	PROM SET (SPECIAL ROM and LSBs)
	U60, 61	21247100	PROM SET (SPARE ROM and LSBs)
A5A16	U70	21233000	Character Generator, DM 8678
	U67	21251200	PROM, Y-Line, SN 74S472N
	U24, 40	21251300	PROM SET, Detector, SN 74S288N
	U14	21251400	PROM, TXA, SN 74S472N
	U37	21251500	PROM, TYA, SN 74S471N
	U51	21251600	PROM, Y-INST, SN 74S472N
	U66	21251700	PROM, X-LINE, SN 74S472N
A5A17	U38	21886100	PROM, (Gain Control)
	U42, 43	21885500	PROM SET (SSG#3, SSG#4)
	U22, 23	21885600	PROM SET (SSG#2, SSG#1)

Table 4-4. Special Replaceable Parts List (Controls and Indicators)

Assembly No.	Reference Designation	Part No.	Description
PS1A1	R2	10648201	Potentiometer, 72XR500
	R5	10648200	Potentiometer, 72XR5K
	R8	10648209	Potentiometer, 72XR20
	S1	10531807	Switch, 7101AQ
	A1	21088800	Resistor, Pwr, Assy
PS1A2	DS1	10620300	Protector, Voltage, B1-A230
	DS2	10614900	Lamp, Neon, A1A
	R53	10544318	Potentiometer, 66XR5K
	R7	10648202	Potentiometer, 72XR10K
	BT1	10710400	Battery, 2.4 VDC, 0.07 AH
PS1A3	F1	10534123	Fuse, 10A, Slo-Blo, 250V
A1	S1/DS1	21298300	Switch Assy, Pwr
A3		10713301	CRT-Scope
A4		21240700	Fan Assy
A5A1/A2	R273	10544309	Potentiometer, 66WR20K
	R33	10544304	Potentiometer, 66WR500
	R53	10544305	Potentiometer, 66WR1K
	R181, 188, 281	10544307	Potentiometer, 66WR5K
	R34, 57, 58	10544312	Potentiometer, 66WR100K
	R3	10544323	Potentiometer, 66XR2K
	R201	10544326	Potentiometer, 66XR50K
	R175	10544321	Potentiometer, 66XR100K
A5A1/A2	R19	10648201	Potentiometer, 72XR500
A5A6	Y1	21349806	Crystal, 16.384 MHz
	U38	10162600	Resistor Pack, 180Ω/390Ω
A5A9	Y1	21338524	Crystal, 3.072 MHz
	U11	10717100	LED Pack, HLMP-6204
	U10	10717101	LED Pack, HLMP-6205
A5A12	DS1	10535601	LED, MV5025
	S1	10619001	Thermostat, 3450-88-205
A5A16	R26, 27	10544110	Potentiometer, 62PR5K
A5A17	C24, 39, 50, 65 70,74	10560203	Capacitor, Trimmer, 15-60pF, 200wvdc
	C78	10560201	Capacitor, Trimmer, 2.5-11pF, 350wvdc
	R38, 40	10665732	Potentiometer, 68XR100K
	R17	10665723	Potentiometer, 68XR200
	R35	10665726	Potentiometer, 68XR2K
	R22	10665727	Potentiometer, 68XR5K
	R7, 60	10665728	Potentiometer, 68XR10K
	R46, 73	10665730	Potentiometer, 68XR25K
A5A18	R1	10648202	Potentiometer, 72XR10K
	DS1	10713201	Audio Indicator, A1-254
A5A19	R1	10544713	Potentiometer, 89PR100K

SECTION V

SD375 OPTIONS THEORY OF OPERATION

5.1 TRANSLATOR

5.1.1 General

The Translator option was incorporated in order to increase the resolution of closely spaced signals on the SD375's crt using the circuitry contained on the A5A4 (Translator) and A5A5 (Translator Filter Output) PWAs. These circuits are employed to select a band of frequencies of interest from the frequency spectrum and translate this frequency band to lower frequencies without loss of phase, amplitude, or frequency accuracy and thereby increase the resolution of closely spaced frequency components. The signal-to-noise ratio of the translated band is also enhanced through translation.

Translation of displayed data is accomplished by using the cursor location as the center frequency of the translated band. Front panel controls and inputs which establish initial conditions for Translator operation include the Zoom factor, Post Filter GAIN factor, and the XLTR (Translator) ON touch control.

Figure 5-5 is a detailed block diagram of the Translator and Translator Filter Output assemblies and has been included along with the following circuit description to facilitate an understanding of the Translator circuitry.

Also included are:

a. Program Flow Charts (Figure 5-6) which appear after paragraph 5.1.6.

b. Program Sequence Tables for Instruction PROMs (Table 5-5) which appear after paragraph 5.1.6.

5.1.2 Detailed Circuit Analysis

The following discussion provides a description of Translator and Filter Output operation as depicted in Figure 5-5.

The translation sequence is initiated by depressing the XLTR ON touch control which results in the cursor register being loaded with the cursor location. This input comes from the Z80 microprocessor on the Control Processor (A5A8). The Z80 microprocessor also sends control inputs as bits 9, 10, and 11 on the the data bus which are decoded to load the center (cursor) frequency location and also load Front Panel Status Inputs to the Status Register (A5A5U74).

The contents of the cursor register are used to increment the Sine/Cosine Address Generator (A5A4U1, 8, 15).

5.1.2.1 Sine Generator

The Sine Generator is composed of three 4-bit control elements (A5A4U1, U8, U15), an adder (U22) to provide the required address offset for selecting the Sine data or Cosine data, and sine PROMs (XSN13 and XSN24) U35 and 48 which provide 16-bit Sine and Cosine values to the multiplier circuitry.

The control elements (A5A4U1, 8, 15) are configured as a 12-bit Accumulator, (Sine Address Generator) that is incremented with the cursor location and clocked by CLK SINE PROM REG and whose function outputs (Fi) are used to address two 1024 word by 8-bit Sine PROMs (U48 and 35) which output the 16-bit sine values for multiplication. The same PROMs generate cosine outputs by means of a 90° offset input. The offset input is accomplished through U22 which adds 256 to the Sine Address Generator output when SEL COS is output from CONTROL PROM (TLR1). Figure 5-1 and Table 5-1 depict sine/cosine product control and sequenced control logic is generated by Control PROMs TLR 1 and TLR 2.

5.1.2.2 Multiplier

The Multiplier (A5A4U61) is a 16 by 16-bit high speed device specifically adapted for digital signal processing.

It accepts sine/cosine constants (X inputs) and the digital data inputs from the Input Signal Conditioner (A5A1 or A5A2) and performs the multiplication to obtain real and imaginary components of the digital data. The products are then loaded into a 16-bit Register File composed of A5A4U36, 42, 49, and 55 by CLK MULT I/O and write buffer ($2^0 2^1$).

The output of the Multiplier is written to the product file by the *WRITE BUFFER* signal. The multiplier product outputs are composed alternately of complexed real and imaginary data words.

Product File Data Word Organization

Product File (Address) 2^1	2^0	Contents
0	0	A Real
0	1	A Imaginary
1	0	B Real
1	1	B Imaginary

The 16-bit complexed word pairs are then written as instructed by the CONTROL PROM to the Translator memory as directed by the Memory Address Multiplexer (MUX).

5.1.3 Memory Address Organization (Write Cycle)

From the Z80 control logic on the Control Processor (A5A8, the MASTER RESET signal is fed to the Translator and through signal conditioning schmitt triggers U5 to clear the 10-bit memory Write Counter (U19, 26, 32) to zero, and to clear the 4-bit Control PROM Address Counter (U44) to zero.

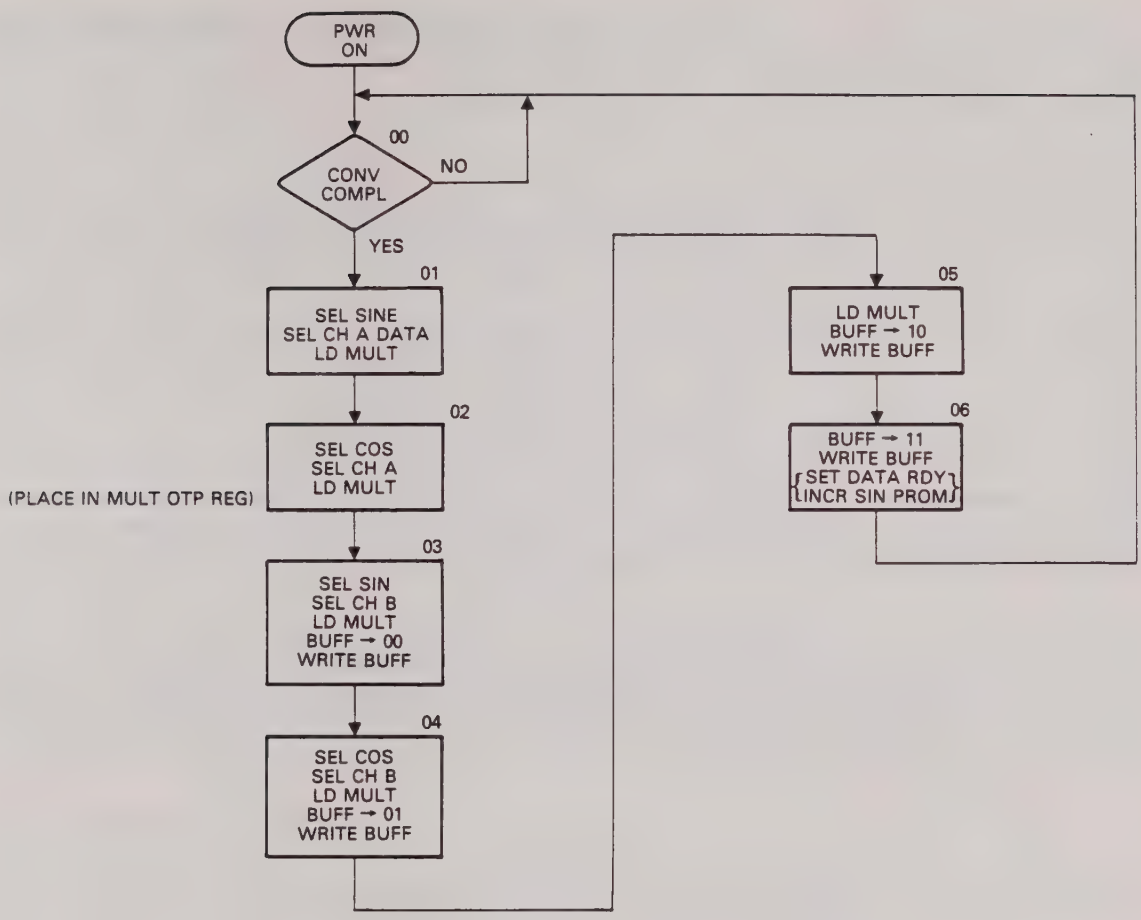


Figure 5-1. Translator Sin/Cos Product Control PROM Program Flow Diagram

Table 5-1. Translator Sin/Cos Product Control PROM (Program) Sequence

	TLR 2										TLR 1									
PROGRAM ADDRESS	JUMP ADDRESS				ϕ 4 CODE		ϕ 3 CODE		SPARE		SEL COS	SEL CHAN B	BUFF RAM 2^1	BUFF RAM 2^0	TEST	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
3	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0
4	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0
5	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0
6	0	0	0	0	1	0	0	1	0	0	0	0	1	1	1	0

The Memory Write Counter operates under control of the Translator Instruction PROM (TLR 4) on the A3A5 PWA (Translator Filter Output). In conjunction with $\phi 4$ clock pulses, a write cycle clock signal (CKWC) is developed and used to increment the Write Counter.

The Write Counter Output is selected by the Address Multiplexer (A5A4U6, 12, 13, 20, 27) when the CTR SELECT bits (2′, 2°) to the A and B inputs are both high (as controlled by the clock code from Translator Instruction PROMs through Decoder A5A5U59). The Address Multiplexer's output is the address in Translator memory at which the complexed word pairs generated by the multiplier are stored.

The Write Counter output is also fed to the Last Address Register (A5A4U39, 45). The last address register is controlled by the Translator Instruction PROMs clock code via Decoder A5A5U59. When LDNR goes high the last count at the Write Counter output is loaded into the Last Address Register. This address is the last address written to the Translator memory plus one (+1).

The Translator continues to write complexed real and imaginary data products to the Register file, read the data from the file, and write it to memory (as controlled by Translator Instruction PROMs on the A5A5 PWA) until a complete ensemble has been processed.

The storage organization is depicted in Figure 5-2. The real and imaginary components of a complexed data word are stored in separate sections of memory as determined by the A10 and A11 memory address bits. These two bits provide the offset for the location in which the imaginary component is written and are determined by TLR6 (Translator Instruction PROM) on the A5A5 PWA. These two bits also separate channel A and B.

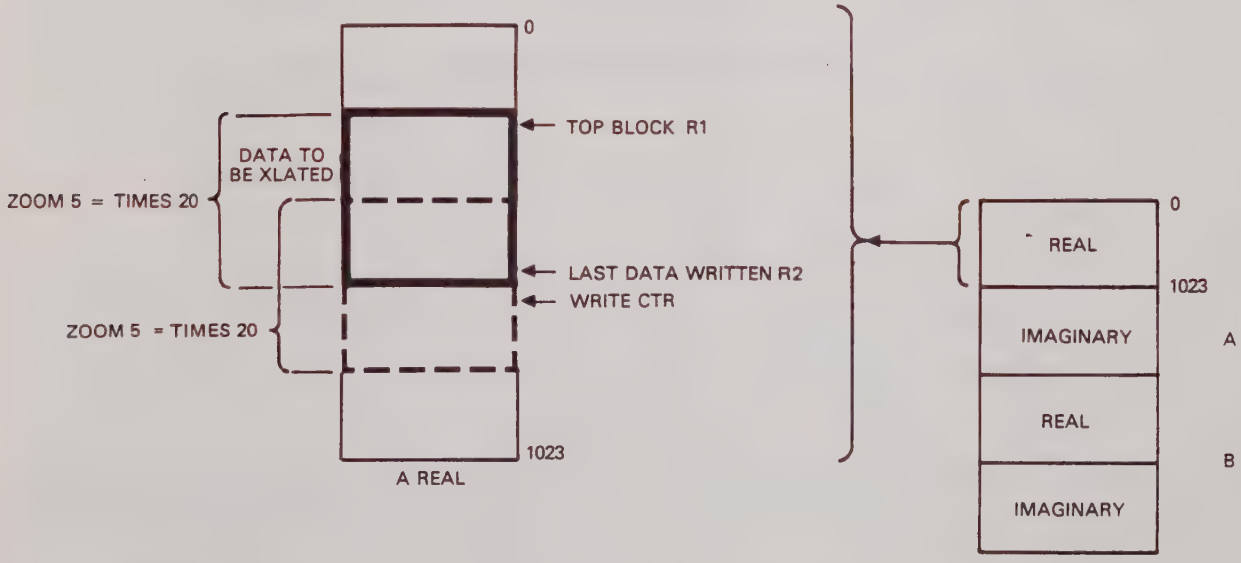


Figure 5-2. Translator Memory Data Storage Organization

5.1.4 Memory Address Organization (Read Cycle)

The Last Address Register stores the last address written into memory plus one +1. Its latched output is the A input to summation network (A5A4U52, 58, 66). The B input to the summation network is an address offset from the Preset PROMs.

The Read cycle is initiated by placing a minus one (−1) offset on the summation network A inputs. This results in a summing network output of LAST ADDRESS REGISTER contents minus one which is loaded to the Read Down Counter when LDDC is received from Translator Instruction PROMs via Clock Code Decoder A5A5U59. The Read Down Counter then points at the last (newest) complexed word stored in Translator memory when the memory write cycle was completed.

The oldest word to be included in the translated output is addressed by the Read Up Counter's (A5A4U53, 59, 67) output. The Read Up Counter is loaded with the LAST ADDR REGISTER contents minus an offset determined by the zoom code from the Status Latch and the Preset Code from the Instruction PROMs to the Preset PROMs (Preset PROMs store offset constants). The Preset PROM output (Address Offset) is summed with the LAST ADDRESS Register Contents and the output is the address of the first word of the block of translated data.

All complexed words stored in Translator memory between the initial locations set into the Read Up and Read Down Counters will be read out as pairs to Register Files R1 and R2. Both Register R1 and R2 are 16-bit latches which are clocked by LDR1 and LDR2 respectively to load the paired complexed words which appear at their inputs.

5.1.5 Translator Output ADDER

All paired complexed words contained in the block between the initial values of the Read Up and Read Down Counters are summed in the 16-bit memory output Adder (A5A4U21).

The summed complexed word pairs are fed to the Translator Filter Output Assembly (A5A5) for processing and then to the Input Memory Assembly (A5A7) for storage.

5.1.6 Translator Filter Output Assembly

The Translator Filter Output serves as a digital filter to eliminate undesired portions of the spectrum which are present after translation. Its primary function is to process the 16-bit summed data word pairs from the Memory Adder on A5A4 to provide a scaled data point for the Input Memory. The translated data point is derived by performing a high speed two's complement multiplication of each paired summation from A5A4 (Translator Assembly) known as $Z(+n) + Z(-n)$ with a predetermined filter coefficient. As each summed input from the Memory Adder is multiplied with it's selected filter coefficient the resultant product is added into the accumulator. The number of summations performed to compute each data point is defined by the Address offset from the Preset PROM and is loaded into the Translator Loop Counter (A5A5U48, 49, and 58) which is counted down by CKLC to zero. After all summed Memory Adder inputs have been processed (*Translator Loop Counter = 0*) the Translator Loop Counter sends TRANS COMPL to the test multiplexer and the Accumulator output is scaled by the shifter circuitry and fed to the Input Memory Assembly (A5A7).

The digital filter operation is initiated when LDCP is decoded from the Instruction PROM Clock Code to load the Coefficient Address Counter with the appropriate address of the first filter coefficient in XCF13 and XCF24 (Filter Coefficient PROMs).

When LDMU is decoded by the clock decoder U59 the Translator Loop Counter is loaded as described in the previous paragraphs to count (and thereby track) the number of summed outputs from the Memory Adder on A5A4 being processed. These summed data word pairs are sequentially loaded into the Multiplier (A5A5U73 with X inputs while the corresponding preselected offset from the filter coefficient PROM is loaded to the Y inputs.

The multiplication is performed and the products are held in the multiplier's output register.

5.1.6.1 Arithmetic Logic Unit (Filter-Adder)

The 16-bit most significant (MS) product and the 10-bits of least significant (LS) product are fed to the Filter-Adder (see A5A5 sheet 4). The Filter-Adder is comprised of an Arithmetic-Logic array with look-ahead-carry generators to perform the running summation of multiplier outputs. The adder is initially cleared by ALU CTL. As each product is generated by the multiplier, it is summed into the Filter-Adder.

The Filter-Adder output is fed back on itself through the 32-bit Adder Output Register (A5A5U1, 6, 30, and 32) and the Accumulator File (A5A5U4, 7, 13, 16, 19, 22, 23 and 47).

5.1.6.2 Filter Output Accumulator File

The Accumulator File is a 32-bit by 4-word register. Its input is the latched 32-bit summation of the arithmetic logic array through the Adder Output Register. The Accumulator File is addressed by the 2-bit File Write ADDR (2^0, 2^1) and the 2-bit FILE READ ADDR (2^0, 2^1) codes to its write and read inputs respectively from Instruction PROM TLR 6. The Accumulator File is selectively written to and is read out to the arithmetic logic array and thereby providing B inputs to the arithmetic logic array for summation with the multiplier product outputs.

The Accumulator File also provides intermediate storage of four (4) processed data points until they are read out to the Input Memory via the Shifter circuitry.

5.1.6.3 Filter Output Shifter

The Filter output Shifter is composed of a 24-bit data point multiplexer (A5A5U3, 20, 21, 28, 29, and 46) an overflow detector (A5A5U11), a 30-bit Programmed Logic Array (FPLA) along with an output adder.

The primary function of the Shifter is to scale the data to compensate for gain that was build into the coefficients used.

The Shift code from the Preset PROM is decoded by the Shifter circuit elements to select which bits will appear at the output. It is decoded by the XSM and XSL Programmed Logic Arrays and used to select the bit ordered output from the Shift Multiplexer (A5A5U3-46). The shift code is a function of the gain code and the zoom code fed from the Status Register. Table 5-2 (Shifter Output Bit Configuration) depicts the gain code, zoom factor, zoom code and the corresponding shift code generated from the Preset PROM. Also depicted are the respective translated data point output bit configurations.

Table 5-2. Shifter Output Bit Configuration

	Zoom Code	000	001	010	011	100	101
Gain Code	Zoom / Gain	2	5	10	20	50	100
00	1	10 → 25 (101)	11 → 26 (100)	12 → 27 (011)	13 → 28 (010)	14 → 29 (001)	15 → 30 (000)
01	2	9 → 24 (110)	10 → 25 (101)	11 → 26 (100)	12 → 27 (011)	13 → 28 (010)	14 → 29 (001)
10	4	8 → 23 (111)	9 → 24 (110)	10 → 25 (101)	11 → 26 (100)	12 → 27 (011)	13 → 28 (010)
11	8		8 → 23 (111)	9 → 24 (110)	10 → 25 (101)	11 → 26 (100)	12 → 27 (011)

A → B Bits selected by shifter to output shift code (PRE 2 PROM)
(XXX)

The (three) type 82S100 FPLAs (Field Programmable Logic Arrays) are designated XOF, XSL, and XSM (A5A5 schematic sheet 5). XOF is programmed to detect overloads and feed an output to the control processor when an overload condition exists. The Data Point multiplexer does a pre-shift of 0 or 8 places (bits). The FPLAs (XSL/XSM) perform the final shift of 0 through 7 places.

The shift code is determined by the zoom and gain factors stored in the Status Register, and the preset code from the TLR 4 Instruction PROM. These three codes are combined to form the address (in PRESET PROMs 1 and 2) of the address offset and the shift code as depicted in Figure 5-3.

The 8-bit address will select the fixed shift and offset constants stored in memory as depicted in Table 5-3 (Loop Constants). The offset constants are fed out to the offset bus and loaded to the following counters when the appropriate clock code from TLR 4 is accessed.

Translator Loop Counter
New Data Counter
Coefficient Address Counter
Read Up Counter
Read Down Counter

The Read Up and Down Counters Offset inputs are combined with last address counts.

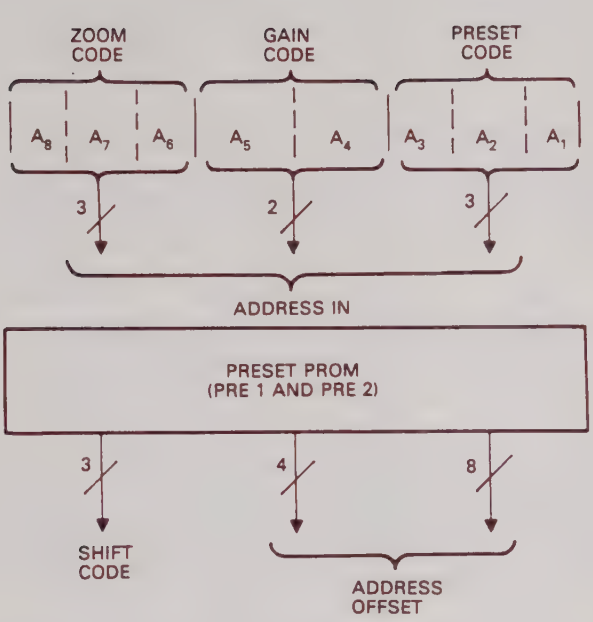


Figure 5-3. Preset PROM Input/Output

5.1.6.4 Clock Generation

Clock codes which generate the various *load* signals from Clock Decoder A5A5U59 and their mnemonics are illustrated in Table 5-4 (Clock Codes).

On the Translator Filter Output Assembly (A5A5) U43 is used to develop four phases of clock pulses for timing the gating various operations within the Translator. The 4ϕ Clock Generator is configured to divide the 16.385 MHz *Multiply Clock* input by four and is loaded with a count of (6) each time the carry is generated (count equals ten (10)). The carry output is fed to U54 which provides the four phases of 61 ns pulses (see Figure 5-4) and used to gate various circuits via U53, 57, 68, and 75. Refer to Figure 5-5 and the A5A5 detailed schematic drawing sheet 2.

5.1.6.5 New Data Counter

The New Data Counter is employed to indicate when a new ensemble is ready for translation. It is loaded with an 8-bit output from Preset PROM (PRE 1) determined by the Z80 status latch. The New Data Counter is decremented by (CKWC), the write counter clock signal to the Translator (A5A4) write counter which causes it to write a new product into Translator memory. When the count reaches zero, as detected by A5A5 U62, it is disabled from counting by START TRANS to its gating inputs. START TRANS is fed to the Test Multiplexer A5A5U63 to enable the loading of Address Counter (A5A5U27, 36) when Instruction PROM Test code is 100 (binary 4). This is the branch instruction to Read Translator Memory.

Table 5-3. Loop Constants

					Output		
					Decimal	PRE 2	PRE 1 (Hex)
Zoom (000)	Gain	Preset	Address	Function	(Constants)	(Shift Code)	Constants
2	1	0	0	COEFF Start	171	5 0	A B
		1	1	#COEF + P/L	11	5 0	0 B
		2	2	#New Values	4 (3)	5 0	0 3
		3	3	UP CTR O/S	−20	D F	E C
		4	4	DN CTR O/S	−1	5 F	F F
2	2	0	8	COEFF Start	171	6 0	A B
		1	9	#COEF + P/L	11	6 0	0 B
		2	10	#New Values	4 (3)	6 0	0 3
		3	11	UP CTR O/S	−20	E F	E C
		4	12	DN CTR O/S	−1	6 F	F F
2	4	0	16	COEFF Start	171	7 0	A B
		1	17	#COEF + P/L	11	7 0	0 B
		2	18	#New Values	4 (3)	7 0	0 3
		3	19	UP CTR O/S	−20	F F	E C
		4	20	DN CTR O/S	−1	7 F	F F
2	8	0	24	COEFF Start	171	7 0	A B
		1	25	#COEF + P/L	11	7 0	0 B
		2	26	#New Values	4 (3)	7 0	0 3
		3	27	UP CTR O/S	−20	F F	E C
		4	28	DN CTR O/S	−1	7 F	F F

Table 5-3. Loop Constants (Continued)

					Output		
					Decimal	PRE 2	PRE 1 (Hex)
Zoom (001)	Gain	Preset	Address	Function	(Constants)	(Shift Code)	Constants
5	1	0	32	COEFF Start	447	4 1	B F
		1	33	#COEF + P/L	26	4 0	1 A
		2	34	#New Values	10 (9)	4 0	0 9
		3	35	UP CTR O/S	−50	C F	C E
		4	36	DN CTR O/S	−1	4 F	F F
5	2	0	40	COEFF Start	447	5 1	B F
		1	41	#COEF + P/L	26	5 0	1 A
		2	42	#New Values	10 (9)	5 0	0 9
		3	43	UP CTR O/S	−50	D F	C E
		4	44	DN CTR O/S	−1	5 F	F F
5	4	0	48	COEFF Start	447	6 1	B F
		1	49	#COEF + P/L	26	6 0	1 A
		2	50	#New Values	10 (9)	6 0	0 9
		3	51	UP CTR O/S	−50	E F	C E
		4	52	DN CTR O/S	−1	6 F	F F
5	8	0	32	COEFF Start	447	7 1	B F
		1	57	#COEF + P/L	26	7 0	1 A
		2	58	#New Values	10 (9)	7 0	0 9
		3	59	UP CTR O/S	−50	F F	C E
		4	60	DN CTR O/S	−1	7 F	F F

Table 5-3. Loop Constants (Continued)

					Output		
					Decimal	PRE 2	PRE 1 (Hex)
Zoom (010)	Gain	Preset	Address	Function	(Constants)	(Shift Code)	Constants
10	1	0	64	COEFF Start	1023	3 F	F F
		1	65	#COEF + P/L	51	3 0	3 3
		2	66	#New Values	20 (9)	3 0	1 3
		3	67	*UP CTR O/S	−100	B F	9 C
		4	68	DN CTR O/S	−1	3 F	F F
10	2	0	72	COEFF Start	1023	4 F	F F
		1	73	#COEF + P/L	51	4 0	3 3
		2	74	#New Values	20 (9)	4 0	1 3
		3	75	*UP CTR O/S	−100	C F	9 C
		4	76	DN CTR O/S	−1	4 F	F F
10	4	0	80	COEFF Start	1023	5 F	F F
		1	81	#COEF + P/L	51	5 0	3 3
		2	82	#New Values	20 (9)	5 0	1 3
		3	83	*UP CTR O/S	−100	D F	9 C
		4	84	DN CTR O/S	−1	5 F	F F
10	8	0	88	COEFF Start	1023	6 F	F F
		1	89	#COEF + P/L	51	6 0	3 3
		2	90	#New Values	20 (9)	6 0	1 3
		3	91	*UP CTR O/S	−100	E F	9 C
		4	92	DN CTR O/S	−1	6 F	F F

*Includes ALU CTL in MSB of PRE 2 used for first 10 sets.

Table 5-3. Loop Constants (Continued)

					Output		
					Decimal	PRE 2	PRE 1 (Hex)
Zoom (011)	Gain	Preset	Address	Function	(Constants)	(Shift Code)	Constants
20	1	0	96	COEFF Start	63	2 0	3 F
		1	97	#COEF + P/L	101	2 0	6 3
		2	98	#New Values	40 (39)	2 0	2 7
		3	99	UP CTR O/S	−200	A F	3 8
		4	100	DN CTR O/S	−1	2 F	F F
20	2	0	104	COEFF Start	63	3 0	3 F
		1	105	#COEF + P/L	101	3 0	6 3
		2	106	#New Values	40 (39)	3 0	2 7
		3	107	UP CTR O/S	−200	B F	3 8
		4	108	DN CTR O/S	−1	3 F	F F
20	4	0	112	COEFF Start	63	4 0	3 F
		1	113	#COEF + P/L	101	4 0	6 3
		2	114	#New Values	40 (39)	4 0	2 7
		3	115	UP CTR O/S	−200	C F	3 8
		4	116	DN CTR O/S	−1	4 F	F F
20	8	0	120	COEFF Start	63	5 0	3 F
		1	121	#COEF + P/L	101	5 0	6 3
		2	122	#New Values	40 (39)	5 0	2 7
		3	123	UP CTR O/S	−200	D F	3 8
		4	124	DN CTR O/S	−1	5 F	F F

Table 5-3. Loop Constants (Continued)

					Output		
					Decimal	PRE 2	PRE 1 (Hex)
Zoom (100)	Gain	Preset	Address	Function	(Constants)	(Shift Code)	Constants
50	1	0	128	COEFF Start	191	1 0	B F
		1	129	#COEF + P/L	251	1 0	F B
		2	130	#New Values	100 (99)	1 0	6 3
		3	131	UP CTR O/S	−500	9 E	0 C
		4	132	DN CTR O/S	−1	1 F	F F
50	2	0	136	COEFF Start	191	2 0	B F
		1	137	#COEF + P/L	251	2 0	F B
		2	138	#New Values	100 (99)	2 0	6 3
		3	139	UP CTR O/S	−500	A E	0 C
		4	140	DN CTR O/S	−1	1 F	F F
50	4	0	144	COEFF Start	191	3 0	B F
		1	145	#COEF + P/L	251	3 0	F B
		2	146	#New Values	100 (99)	3 0	6 3
		3	147	UP CTR O/S	−500	B E	0 C
		4	148	DN CTR O/S	−1	3 F	F F
50	8	0	152	COEFF Start	191	4 0	B F
		1	153	#COEF + P/L	251	4 0	F B
		2	154	#New Values	100 (99)	4 0	6 3
		3	155	UP CTR O/S	−500	C E	0 C
		4	156	DN CTR O/S	−1	4 F	F F

Table 5-3. Loop Constants (Continued)

					Output		
					Decimal	PRE 2	PRE 1 (Hex)
Zoom (101)	Gain	Preset	Address	Function	(Constants)	(Shift Code)	Constants
100	1	0	160	COEFF Start	511	0 1	F F
		1	161	#COEF + P/L	501	0 1	F 5
		2	162	#New Values	200 (199)	0 0	C 7
		3	163	UP CTR O/S	−1000	8 C	1 8
		4	164	DN CTR O/S	−1	0 F	F F
100	2	0	168	COEFF Start	511	1 1	F F
		1	169	#COEF + P/L	501	1 1	F 5
		2	170	#New Values	200 (199)	1 0	C 7
		3	171	UP CTR O/S	−1000	9 C	1 8
		4	172	DN CTR O/S	−1	1 F	F F
100	4	0	176	COEFF Start	511	2 1	F F
		1	177	#COEF + P/L	501	2 1	F 5
		2	178	#New Values	200 (199)	2 0	C 7
		3	179	UP CTR O/S	−1000	A C	1 8
		4	180	DN CTR O/S	−1	2 F	F F
100	8	0	184	COEFF Start	511	3 1	F F
		1	185	#COEF + P/L	501	3 1	F 5
		2	186	#New Values	200 (199)	3 0	C 7
		3	187	UP CTR O/S	−1000	B C	1 8
		4	188	DN CTR O/S	−1	3 F	F F

Table 5-3. Loop Constants (Continued)

					Output		
					Decimal	PRE 2	PRE 1 (Hex)
Zoom (110)	Gain	Preset	Address	Function	(Constants)	(Shift Code)	Constants
2	1	0	192	COEFF Start	51	5 0	3 3
		1	193	#COEF + P/L	8	5 0	0 8
		2	194	#New Values	5 (3)	5 0	0 3
		3	195	UP CTR O/S	−14	D F	F 2
		4	196	DN CTR O/S	−1	5 F	F F
2	2	0	200	COEFF Start	51	6 0	3 3
		1	201	#COEF + P/L	8	6 0	0 8
		2	202	#New Values	5 (3)	6 0	0 3
		3	203	UP CTR O/S	−14	E F	F 2
		4	204	DN CTR O/S	−1	6 F	F F
2	4	0	208	COEFF Start	51	7 0	3 3
		1	209	#COEF + P/L	8	7 0	0 8
		2	210	#New Values	5 (3)	7 0	0 3
		3	211	UP CTR O/S	−14	F F	F 2
		4	212	DN CTR O/S	−1	7 F	F F
2	8	0	216	COEFF Start	51	7 0	3 3
		1	217	#COEF + P/L	8	7 0	0 8
		2	218	#New Values	5 (3)	7 0	0 3
		3	219	UP CTR O/S	−14	F F	F 2
		4	220	DN CTR O/S	−1	7 F	F F

Table 5-4. Clock Codes

Clock Code	Generation	Mnemonic
0 0 0	NOP	
0 0 1	LD New Addr Reg/New Data Loop Ctr	LDNR
0 1 0	LD Up Ctr/Clr Accum	LDUC
0 1 1	LD Dn Ctr	LDDC
1 0 0	LD Coeff Ctr	LDCF
1 0 1	LD Trans Loop Ctr	LDTL
1 1 0	LD Trans Data → Analyzer	LDOR
1 1 1	(Xlator Data Ready)	

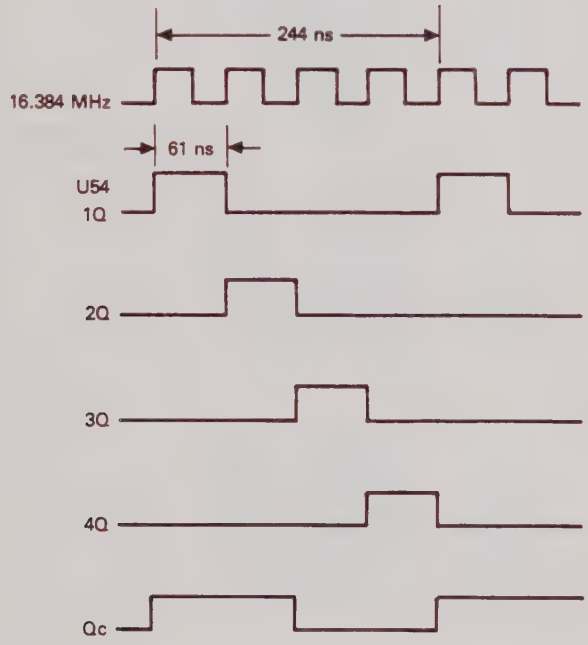


Figure 5-4. Four Phase Clock

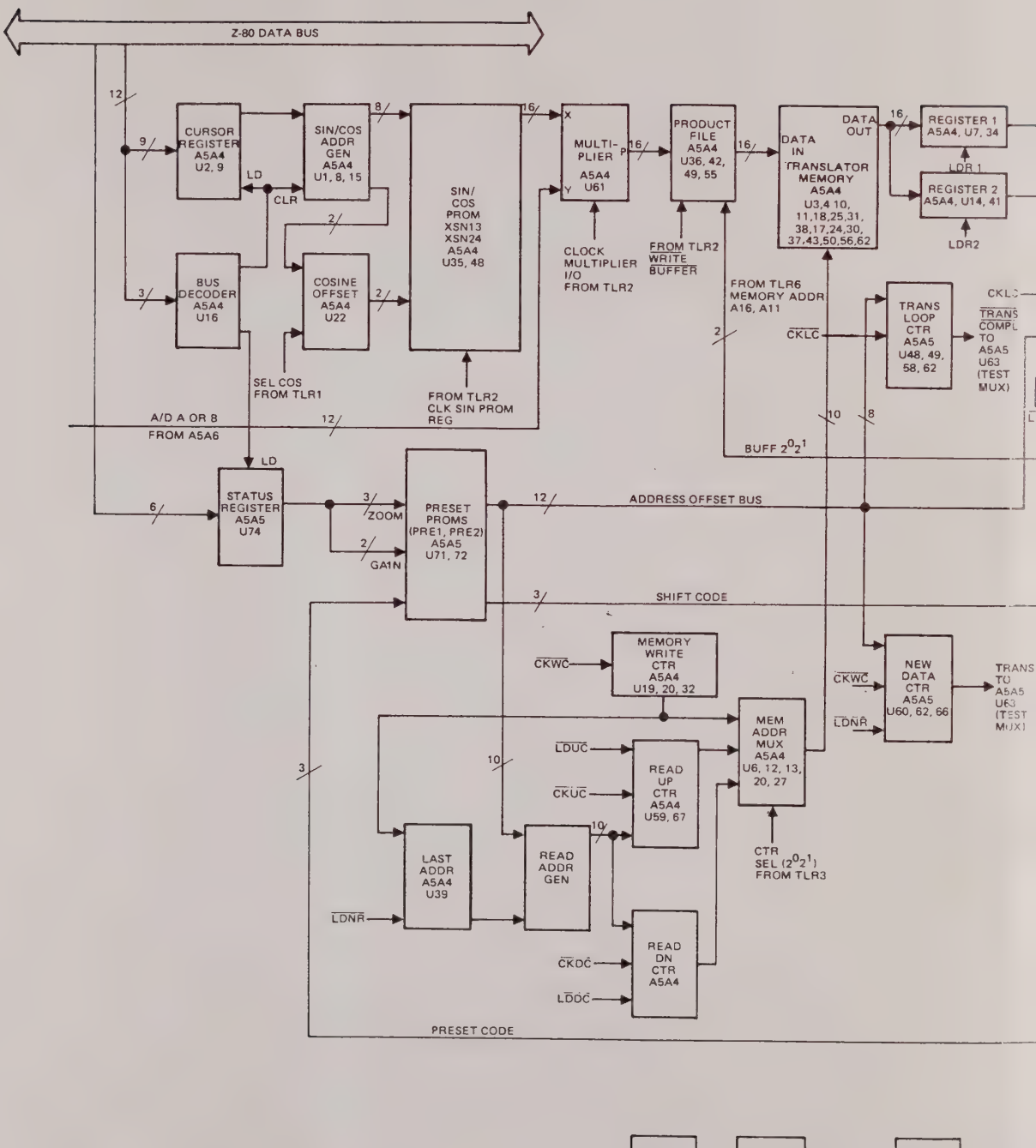
5.1.6.6 Translator Loop Counter

The Translate Loop Counter (A5A5U48, 49, 58) is employed to signal the completion of a translated window. When the number of data points required to generate a complexed pair to the Input Memory has been processed, the Loop Counter will have decremented to zero from the offset initially loaded. The count initially loaded into the Loop Counter is the binary number of complexed word pairs required times the number of points on the translated window.

The Loop Counter is decremented simultaneously with each multiplication performed by A5A5U73. When it reaches zero, its MIN/MAX outputs all reach high levels. The output of NAND gate A5A5U62 goes low and is inverted to disable the counter by placing a high level on the LOAD inputs. The positive pulse generated (TRANS COMPL) is fed to the machine state Test Multiplexer A5A5U63 which yields a low output to load the branch address from Instruction PROM (TLR 5).

Table 5-5. Translator and Translator Filter Output Instruction and Control (Program) Sequence

	TLR 6						TLR 5									TLR 4									TLR 3								
PROGRAM ADDRESS	CLOCK	WFE	FILE WA		FILE RA		MEM SEG		BRANCH ADDRESS					CTR PRESET			BUFF READ		CLOCK			TEST							WRITE INP FILE	AC CLR	READ	WRITE
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0
2	0	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0
3	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
7	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
8	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
9	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
10	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
11	0	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
12	0	1	1	1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
13	0	1	0	0	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
15	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
17	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	1
18	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1
20	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	1
21	0	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1
22	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	1
23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
28	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
29	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
30	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0	1
31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0


Z-80 DATA BUS
CURSOR REGISTER A5A4 U2, 9
SIN/COS ADDR GEN A5A4 U1, 8, 15
LD
CLR
SIN/ COS PROM XSN13 XSN24 A5A4 U35, 48
MULTI-PLIER A5A4 U61
PRODUCT FILE A5A4 U36, 42, 49, 55
DATA IN TRANSLATOR MEMORY A5A4 U3,4 10, 11,18,25,31, 38,17,24,30, 37,43,50,56,62
DATA OUT
REGISTER 1 A5A4, U7, 34
REGISTER 2 A5A4, U14, 41
LDR 1
LDR2
BUS DECODER A5A4 U16
COSINE OFFSET A5A4 U22
CLOCK MULTIPLIER I/O FROM TLR2
FROM TLR2 WRITE BUFFER
FROM TLR6 MEMORY ADDR A16, A11
TRANS LOOP CTR A5A5 U48, 49, 58, 62
CKLC
TRANS COMPL TO A5A5 U63 (TEST MUX)
SEL COS FROM TLR1
FROM TLR2 CLK SIN PROM REG
A/D A OR 8 FROM A5A6
BUFF $2^0 2^1$
STATUS REGISTER A5A5 U74
ZOOM
GAIN
PRESET PROMS (PRE1, PRE2) A5A5 U71, 72
ADDRESS OFFSET BUS
SHIFT CODE
MEMORY WRITE CTR A5A4 U19, 20, 32
CKWC
NEW DATA CTR A5A5 U60, 62, 66
LDNR
TRANS TO A5A5 U63 (TEST MUX)
MEM ADDR MUX A5A4 U6, 12, 13, 20, 27
LDUC
CKUC
READ UP CTR A5A4 U59, 67
CTR SEL ($2^0 2^1$) FROM TLR3
LAST ADDR A5A4 U39
READ ADDR GEN
READ DN CTR A5A4
CKDC
LDDC
PRESET CODE
MULT CLK
4 PHASE CLK CTR A5A5 U43
4 PHASE LATCH A5A5 U54
Ø3
Ø4
Ø1/Ø2 GATES A5A5 U53, 75
EFC TO
LDR2
LDR1
CKLC

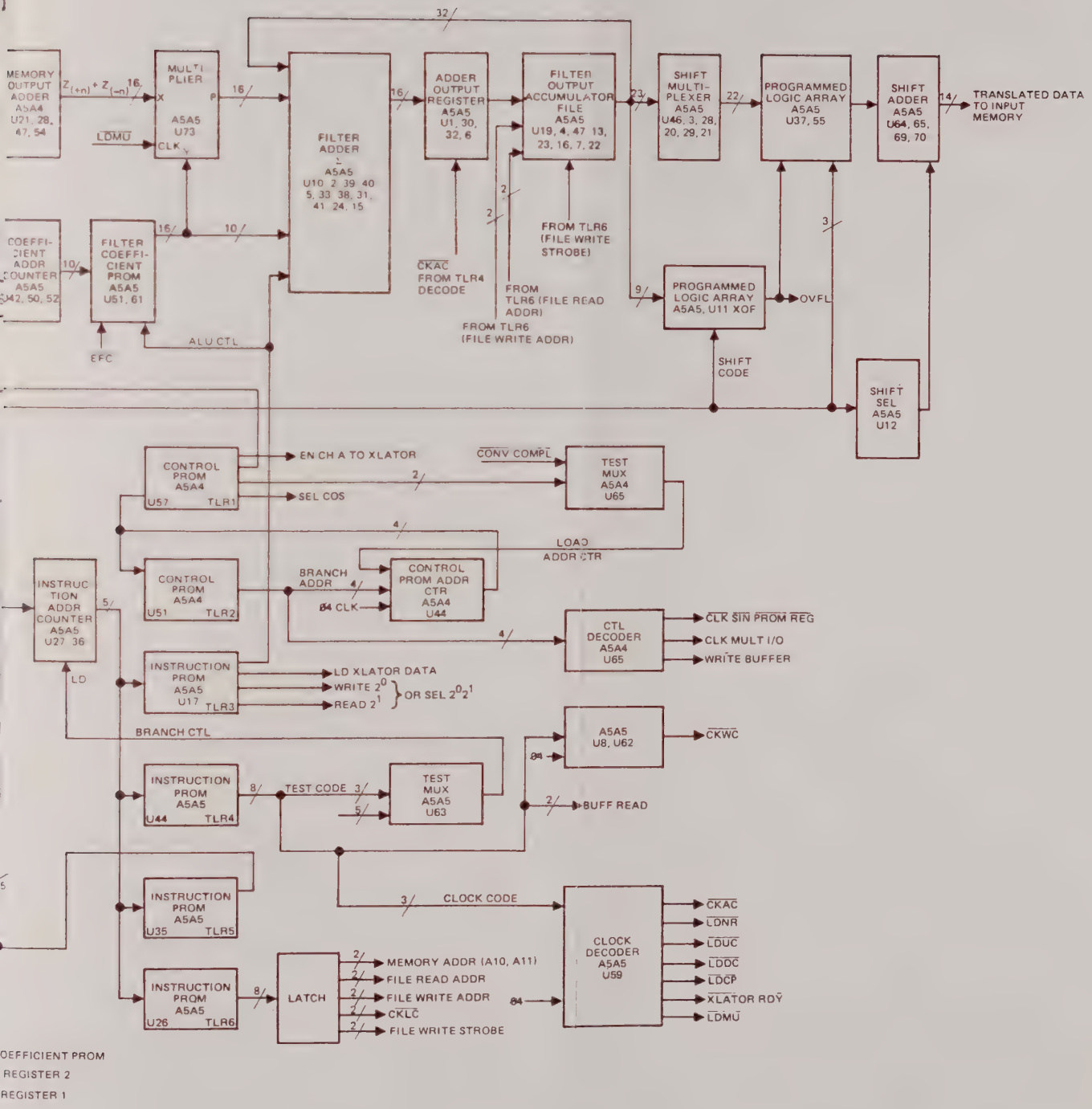


Figure 5-5. Translator (A5A4) and Translator Filter Output (A5A5) Detailed Block Diagram

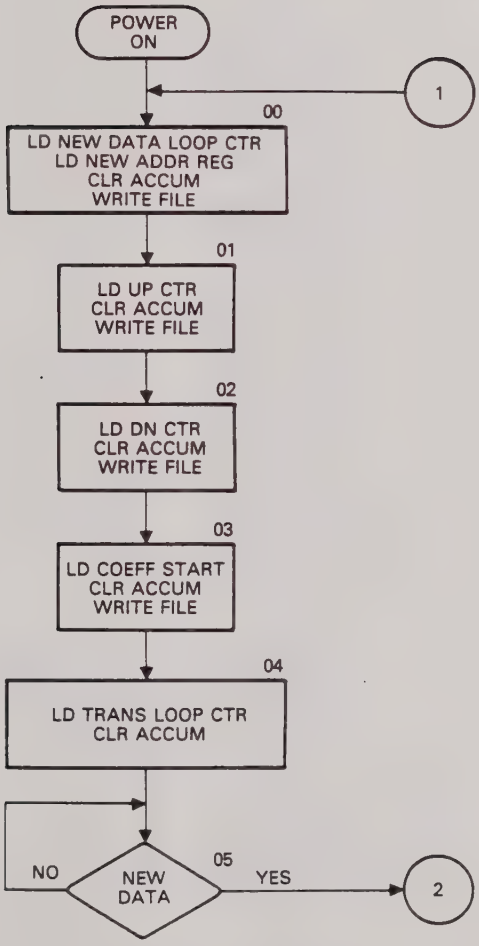


Figure 5-6. Translator and Translator Filter Output Program Flow Diagram (Sheet 1 of 3)

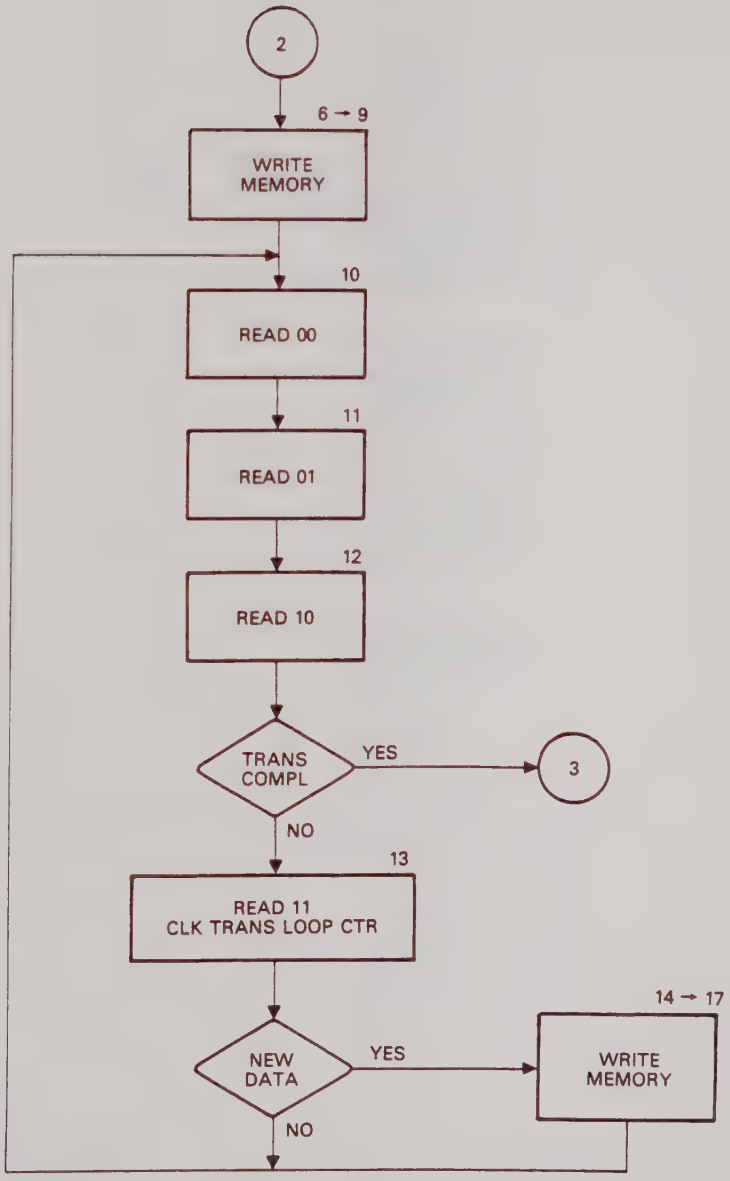


Figure 5-6. Translator and Translator Filter Output Program Flow Diagram (Sheet 2 of 3)

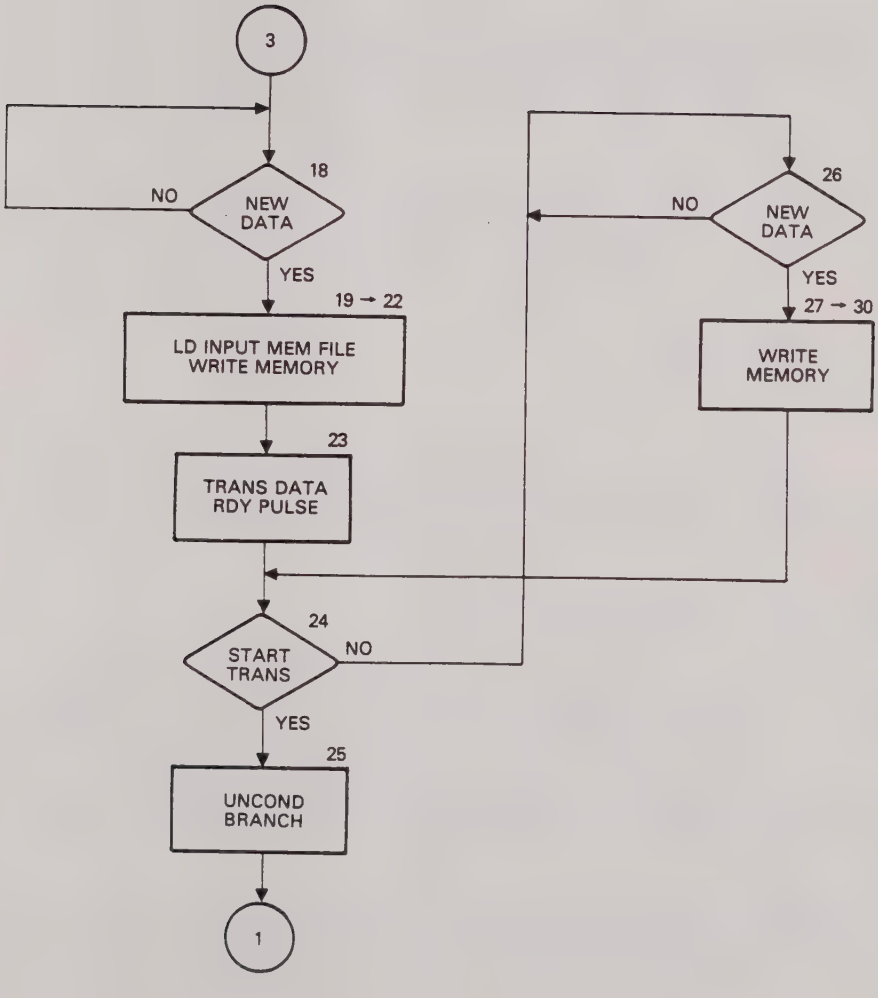


Figure 5-6. Translator and Translator Filter Output Program Flow Diagram (Sheet 3 of 3)

5.2 1/3 AND 1/1 OCTAVE (-2 OPTION)

5.2.1 General Description

The "-2" option to the SD375 provides 1/3 octave, 1/1 octave, and dual channel narrowband analysis capabilities into the Dynamic Analyzer II. Selection of the 1/3 or 1/1 octave display modes is accomplished by using the spectrum group front panel touch controls as detailed in the User's Instruction Manual.

The "-2" option employs a single pass parallel process for data acquisition and synthesis of 1/3 and 1/1 octave spectra. Each spectrum is synthesized from the same segment of the data record stored in memory to ensure that displayed data and measurements accurately portrays the impulse parameters of the signal source.

There are numerous differences in the hardware employed by the SD375-2 (1/3 octave) option, and other instruments which are not configured as such. These differences will be covered here in Section 5. References to Section 2 are made where there are no differences in operating principles.

5.2.2 Input Signal Conditioning

5.2.2.1 General

In order to synthesize 1/3 octave data employing single pass parallel data acquisition new input signal conditioning assemblies are used. These circuits operate in essentially the same manner as described in Section 2 except as described below.

5.2.2.2 Analog Signal Normalization and Filtering

The Analog Input Signal is applied to either the Input A or B BNC connector and is processed as described in Section 2 through input coupling, common mode rejection, and variable gain amplifiers to the low pass filters. The Channel A Low-Pass Filter (LPF) is used for both narrowband normalization of analog inputs (normal operation) and normalization of high group (signals above the 1/3 octave band center frequency) input signals. The Channel B LPF processes the low group (signals below the 1/3 octave band center frequency).

The Z80 microprocessor supplies the hexidecimal analysis range code to the input signal conditioners A and B via Analysis Range Latch (U26) on the Timing & Control (A5A6) board. This 5-bit code forms the address of the desired ranging bits in the Analysis Range PROMs (U65) on A5A1 and A5A2 (Signal Conditioners) which serve to (1) set the digital switches within the LPF's to establish the corner (cutoff) frequencies for the selected range, and (2) set relays to route Channel A and/or B data in agreement with input source selections made using the front panel Display Group Dual/Single and Upper/Lower touch controls.

The Input Signal Conditioners (A5A1 and A5A2) are electrically identical assemblies with one minor exception. Units equipped with the 1/3 octave option have A5A1-B31 grounded. This necessitates that A5A1 not be interchanged with A5A2 in order that the unit function normally in 1/3 octave.

Figure 5-7 is a simplified block diagram depicting the interconnection of input signal conditioners A and B. When the dual display mode is selected, the Channel A and B signal conditioners operate as separate dual channel analog signal conditioners. When the single/upper or lower display controls are selected in conjunction with 1/3 or 1/1 octave Spectrum touch controls, the upper display represents displayed Channel A 1/3 or 1/1 octave upper group data while the lower display represents Channel B.

5.2.3 1/3 Octave Analysis Ranging

The "-2" option has seven 1/3 octave analysis ranges including the 2 kHz through 100 kHz spectrum (2, 4, 5, 10, 20, 50 and 100 kHz). Each range is divided into 10 octave (bands) whose center frequencies, sample frequencies, corner frequencies, band numbers, and inclusive cell locations are depicted in Table 5-6.

One-third octave analysis range decoding circuits are located on both the A5A1 and A5A2 assemblies. These circuits accept the latched Z80 range data from A5A6U26 and provide controls for generation and selection of Channel A and B sample frequencies employed in digitizing high group and low group data, respectively.

Normal narrowband ranges and associated range codes are depicted in Table 5-7. This table is extended to include the 1/3 octave bit configuration.

The 1/3 octave analysis range decoding circuitry (located on A5A6 drawing number 21837000) generates the following signals:

RANGE > 5 kHz
AR 100 kHz TO A1
THIRD OCTAVE
AR 100 kHz TO A2

These signals control the configuration of the input signal conditioners for 1/3 octave operation.

The 1/3 Octave Analysis Range Decoders examine the state of bits 4 and 5 of the range code (Z80 data bus bits D0 through D4). The only time both bits are 1 (set) is in 1/3 octave.

The THIRD OCTAVE and RANGE > 5 kHz signals are fed to the Input Memory Assembly (A5A7) Logic Controller as test selector inputs to U21. When these signals are both true a branch instructor is executed with results in the high speed transfer of Memory Data via the Control Processor DMA (Direct Memory Access) from Input Memory to Processor Memory (M1). This process is incorporated to ensure that the complete ensemble of the signal being analyzed is not truncated by new data being processed to input memory. This transfer is primarily accomplished to preserve high group data (which is processed at a faster rate than low group data).

5.2.4 Input Memory Assembly

5.2.4.1 Display Control

The hardware which controls the input signal conditioning circuit configurations for 1/3 octave analysis is contained on the Input Memory Assembly (A5A7). This circuitry includes A5A7U53 and U38 (see drawing number 21046500 sheet 3). The front-panel DUAL and UPPER touch control inputs are OR'd with THIRD OCTAVE to control relay drivers A5A1 or A2Q19 with the *A to Both* or *B to Both* drive pulses.

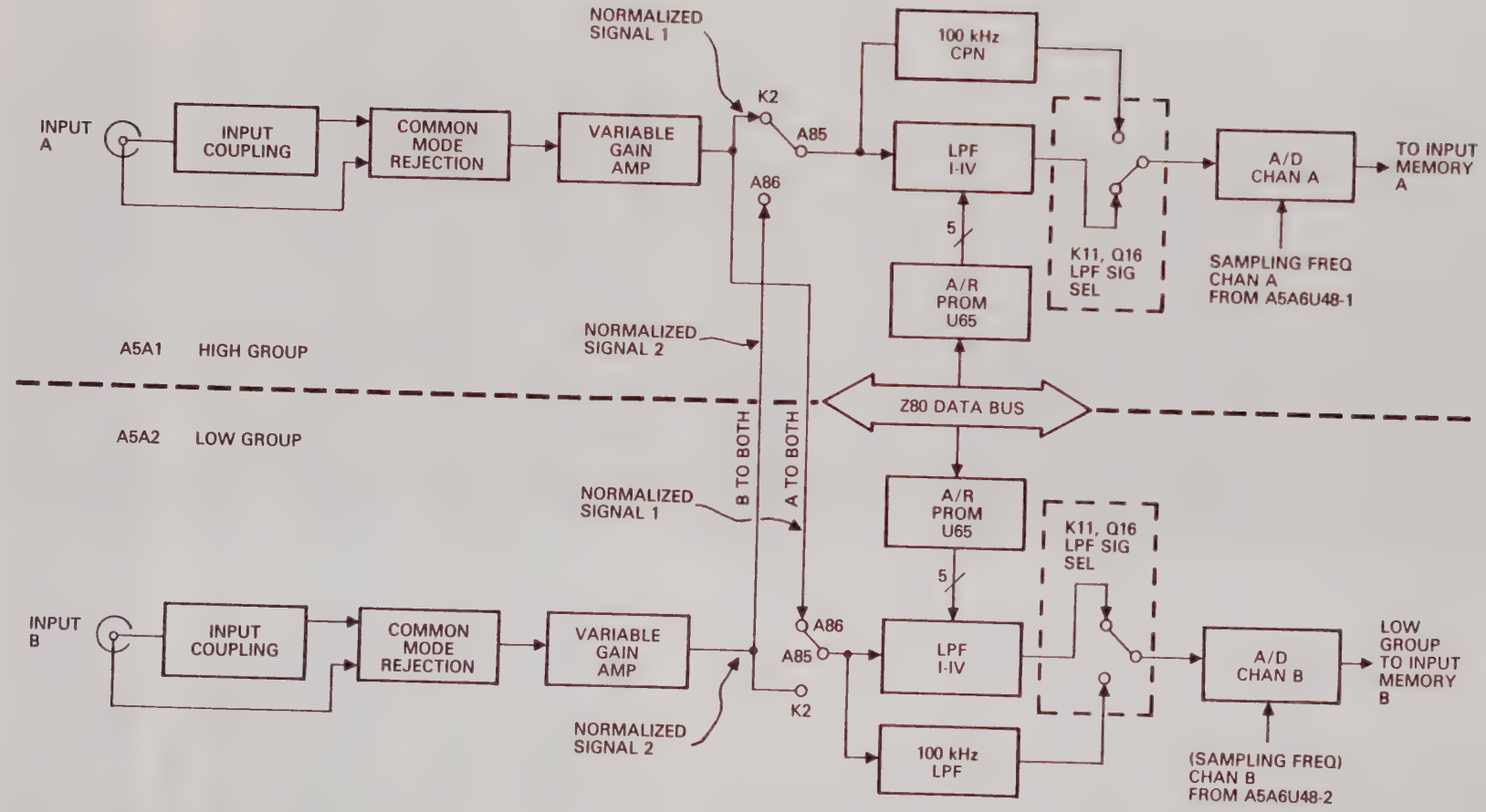


Figure 5-7. Input Signal Conditioners A & B Simplified Interconnect Diagram (1/3, 1/1 Octave)

Table 5-6. One-Third (1/1) Octave Bands

1/3 Octave Analysis Range = 1.25 kHz

Band No.	Band Center Frequency (C.F.)	C.F. $\times 2^{-1/6}$	C.F. $\times 2^{1/6}$	Low Cell	High Cell	Low Frequency	High Frequency
Δf = 5 Hz High Group		Filter Corner = 2 kHz		Fs = 5.12 kHz			
31	1250	1113.6	1403.1	224	287	1117.5	1437.5
30	992.3	883.9	1113.6	178	223	887.5	1117.5
29	787.5	701.5	883.9	141	177	702.5	887.5
28	625	556.8	701.5	112	140	557.5	702.5
27	496.1	442	556.8	89	111	442.5	557.5
26	393.7	350.8	442	71	88	352.5	442.5
25	312.5	278.4	350.8	56	70	277.5	352.5
24	248	221	278.4	45	55	222.5	277.5
23	196.9	175.4	221	36	44	177.5	222.5
22	156.3	139.2	175.4	28	35	137.5	177.5
21	124	110.5	139.2	23	27	112.5	137.5
20	98.4	87.7	110.5	18	22	87.5	112.5
19	78.1	69.6	87.7	15	17	72.5	87.5
18	62	55.2	69.6	12	14	57.5	72.5
17	49.2	43.9	55.2	9	11	42.5	57.5
Δf = 0.16 Low Group		Filter Corner = 50 Hz		Fs = 160 Hz			
16	40	35.6	43.9	224	287	34.9	44.9
15	31.75	28.3	35.6	178	223	27.7	34.9
14	25.2	22.5	28.3	141	177	21.9	27.7
13	20	17.8	22.5	112	140	17.4	21.9
12	15.9	14.14	17.8	89	111	13.8	17.4
11	12.60	11.22	14.14	71	88	11.02	13.8
10	10.00	8.91	11.22	56	70	8.7	11.02
9	7.94	7.07	8.91	45	55	6.95	8.7
8	6.30	5.61	7.07	36	44	5.55	6.95
7	5	4.45	5.61	28	35	4.3	5.55
6	3.97	3.54	4.45	23	27	3.52	4.3
5	3.15	2.81	3.54	18	22	2.73	3.52
4	2.5	2.23	2.81	15	17	2.27	2.73
3	1.98	1.77	2.23	12	14	1.8	2.27
2	1.57	1.40	1.77	9	11	1.33	1.8

Table 5-6. One-Third (1/1) Octave Bands (Continued)

1/3 Octave Analysis Range = 2.5 kHz

Band No.	Band Center Frequency (C.F.)	C.F. $\times 2^{-1/6}$	C.F. $\times 2^{1/6}$	Low Cell	High Cell	Low Frequency	High Frequency
Δf = 7.81 High Group		Filter Corner = 3 kHz		Fs = 8 kHz			
34	2.5K	2227.3	2806.2	286	359	2230.5	2808.6
33	1984.3	1767.8	2227.3	227	285	1769.5	2230.5
32	1574.9	1403.1	1767.8	180	226	1402.3	1769.5
31	1250	1113.6	1403.1	143	179	1113.9	1402.3
30	992.1	883.9	1113.6	114	142	886.7	1113.9
29	787.5	701.5	883.9	90	113	699.2	886.7
28	625	556.8	701.5	72	89	558.6	699.2
27	496.1	441.9	556.8	57	71	441.4	558.6
26	393.7	350.8	441.9	45	56	347.7	441.4
25	312.5	278.4	350.8	36	44	277.3	347.7
24	248	221	278.4	29	35	222.7	277.3
23	196.9	175.4	221	23	28	175.8	222.7
22	156.25	139.2	175.4	18	22	136.7	175.8
21	124	110.5	139.2	15	17	113.3	136.7
20	98.4	87.7	110.5	12	14	89.8	113.3
Δf = 0.24 Low Group		Filter Corner = 90 Hz		Fs = 250 Hz			
19	80	71.3	87.7	286	359	69.7	87.8
18	63.5	56.6	71.3	227	285	55.3	69.7
17	50.4	44.9	56.6	180	226	43.8	55.3
16	40	35.6	44.9	143	179	34.9	43.8
15	31.75	28.3	35.6	114	142	27.7	34.9
14	25.2	22.5	28.3	90	113	21.9	27.7
13	20	17.8	22.5	72	89	17.5	21.9
12	15.9	14.1	17.8	57	71	13.8	17.5
11	12.6	11.2	14.1	45	56	10.9	13.8
10	10	8.9	11.2	36	44	8.7	10.9
9	7.9	7.1	8.9	29	35	7	8.7
8	6.3	5.6	7.1	23	28	5.5	7
7	5.0	4.5	5.6	18	22	4.3	5.5
6	4	3.5	4.5	15	17	3.5	4.3
5	3.15	2.8	3.5	12	14	2.8	3.5

Table 5-6. One-Third (1/1) Octave Bands (Continued)

1/3 Octave Analysis Range = 5 kHz

Band No.	Band Center Frequency (C.F.)	C.F. $\times 2^{-1/6}$	C.F. $\times 2^{1/6}$	Low Cell	High Cell	Low Frequency	High Frequency
Δf = 15.625 High Group		Filter Corner = 6 kHz		Fs = 16 kHz			
37	5 K	4454.9	5612.3	286	359	4460.9	5617.2
36	3968.5	3535.5	3535.5	227	285	3539.1	4460.9
35	3149.8	2806.2	2806.2	180	226	2804.7	3539.1
34	2500	2227.2	2227.2	143	179	2226.6	2804.7
33	1984.3	1767.8	1767.8	114	142	1773.4	2226.6
32	1574.9	1403.1	1403.1	90	113	1398.4	1773.4
31	1250	1113.6	1113.6	72	89	1117.2	1398.4
30	992.1	883.9	883.9	57	71	882.8	1117.2
29	787.5	701.5	701.5	45	56	695.3	882.8
28	625	556.8	556.8	36	44	554.7	695.3
27	496.1	441.9	441.9	29	35	445.3	554.7
26	393.7	350.8	350.8	23	28	351.6	445.3
25	312.5	278.4	278.4	18	22	273.4	351.6
24	248	221	221	15	17	226.6	273.4
23	196.9	175.4	175.4	12	14	179.7	226.6
Δf = 0.488 Low Group		Filter Corner = 180 Hz		Fs = 500 Hz			
22	160 Hz	142.5	179.6	286	359	139.4	175.5
21	127	113.1	142.5	227	285	110.6	139.4
20	100.8	89.8	113.1	180	226	87.7	110.6
19	80	71.3	89.8	143	179	69.6	87.7
18	63.5	56.6	71.3	114	142	55.4	69.6
17	50.4	44.9	56.6	90	113	43.7	55.4
16	40	35.6	44.9	72	89	34.9	43.7
15	31.7	28.3	35.6	57	71	27.6	34.9
14	25.2	22.4	28.3	45	56	21.7	27.6
13	20	17.8	22.4	36	44	17.3	21.7
12	15.9	14.1	17.8	29	35	13.9	17.3
11	12.6	11.2	14.1	23	28	11	13.9
10	10	8.9	11.2	18	22	8.5	11
9	7.9	7.1	8.9	15	17	7.1	8.5
8	6.3	5.6	7.1	12	14	5.6	7.1

Table 5-6. One-Third (1/1) Octave Bands (Continued)

1/3 Octave Analysis Range = 10 kHz

Band No.	Band Center Frequency (C.F.)	C.F. $\times 2^{-1/6}$	C.F. $\times 2^{1/6}$	Low Cell	High Cell	Low Frequency	High Frequency
Δf = 31.25 High Group		Filter Corner = 12K		Fs = 32 kHz			
40	10K	8909	11224.6	286	359	8921.9	11234.4
39	7937	7071.1	8909	227	285	7078.1	8921.9
38	6299.6	5612.3	7071.1	180	226	5609.4	7078.1
37	5K	4454.5	5612.3	143	179	4453.1	5609.4
36	3968.5	3535.5	4454.5	114	142	3546.9	4453.1
35	3149.8	2806.2	3535.5	90	113	2796.9	3546.9
34	2500	2227.2	2806.2	72	89	2234.4	2796.9
33	1984.3	1767.8	2227.2	57	71	1765.6	2234.4
32	1574.9	1403.1	1767.8	45	56	1390.6	1765.6
31	1250	1113.6	1403.1	36	44	1109.4	1390.6
30	992.1	883.9	1113.6	29	35	890.6	1109.4
29	787.5	701.5	883.9	23	28	703.1	890.6
28	625	556.8	701.5	18	22	546.9	703.1
27	496.1	441.9	556.8	15	17	453.1	546.9
26	393.7	350.8	441.9	12	14	359.4	453.1
Δf = 0.9766 Low Group		Filter Corner = 370		Fs = 1 KHz			
25	315	280.6	353.6	286	359	278.8	351.1
24	250	222.74	280.6	227	285	221.2	278.8
23	198.4	176.79	222.74	180	226	175.3	221.2
22	157.5	140.32	176.79	143	179	139.2	175.3
21	125	111.37	140.32	114	142	110.8	139.2
20	99.2	88.39	111.37	90	113	87.4	110.8
19	78.75	70.16	88.39	72	89	69.8	87.4
18	62.5	55.68	70.16	57	71	55.2	69.8
17	49.6	44.2	55.68	45	56	43.5	55.2
16	39.375	35.08	44.2	36	44	34.7	43.5
15	31.25	27.84	35.08	29	35	27.8	34.7
14	24.8	22.1	27.84	23	28	22	27.8
13	19.7	17.54	22.1	18	22	17.1	22
12	15.6	13.92	17.54	15	17	14.2	17.1
11	12.4	11.05	13.92	12	14	11.2	14.2

Table 5-6. One-Third (1/1) Octave Bands (Continued)

1/3 Octave Analysis Range = 20 kHz

Band No.	Band Center Frequency (C.F.)	C.F. $\times 2^{-1/6}$	C.F. $\times 2^{1/6}$	Low Cell	High Cell	Low Frequency	High Frequency
Δf = 62.5 Hz High Group		Filter Corner = 25 kHz		Fs = 64 kHz			
43	20K	17818	22449	286	359	17843.75	22468.75
42	15874	14142	17818	227	285	14156.25	17843.75
41	12599	11225	14142	180	226	11218.75	14156.25
40	10K	8909	11225	143	179	8906.25	11218.75
39	7937	7071	8909	114	142	7093.75	8906.25
38	6300	5612	7071	90	113	5593.75	7093.75
37	5K	4454	5612	72	89	4468.75	5593.75
36	3969	3536	4454	57	71	3531.25	4468.75
35	3150	2806	3536	45	56	2781.25	3531.15
34	2.5K	2227	2806	36	44	2218.75	2781.25
33	1984	1768	2227	29	35	1781.25	2218.75
32	1575	1403	1768	23	28	1406.25	1781.25
31	1250	1114	1403	18	22	1093.75	1406.25
30	992	884	1114	15	17	906.25	1093.75
29	787	702	884	12	14	718.75	906.25
Δf = 2.5 Hz Low Group		Filter Corner = 1 kHz		Fs = 2.56 kHz			
28	630	561.3	707.2	224	287	558.75	718.75
27	500	445	561.3	178	223	443.75	558.75
26	396.9	353.6	445	141	177	351.25	443.75
25	315	280.6	353.6	112	140	278.75	351.25
24	250	222.7	280.6	89	111	221.25	278.75
23	198.4	176.8	222.7	71	88	176.25	221.25
22	157.5	140.3	176.8	56	70	138.75	176.25
21	125	111.4	140.3	45	55	111.25	138.75
20	99.2	88.4	111.4	36	44	88.75	111.25
19	78.75	70.2	88.4	28	35	68.75	88.75
18	62.5	55.7	70.2	23	27	56.25	68.75
17	49.6	44.2	55.7	18	22	43.75	56.25
16	39.4	35.1	44.2	15	17	36.25	43.75
15	31.25	27.8	35.1	12	14	28.75	36.25
14	24.8	22.1	27.8	9	11	21.25	28.75

Table 5-6. One-Third (1/1) Octave Bands (Continued)

1/3 Octave Analysis Range = 40 kHz

Band No.	Band Center Frequency (C.F.)	C.F. $\times 2^{-1/6}$	C.F. $\times 2^{1/6}$	Low Cell	High Cell	Low Frequency	High Frequency
Δf = 125 Hz High Group		Filter Corner = 50 kHz		Fs = 128 kHz			
46	40K	35636	44898	286	359	35687.5	44937.5
45	31748	28284	35636	227	285	28312.5	35687.5
44	25198	22449	28284	180	226	22437.5	28312.5
43	20K	17818	22449	143	179	17812.5	22437.5
42	15874	14142	17818	114	142	14187.5	17812.5
41	12599	11225	14142	90	113	11187.5	14187.5
40	10K	8909	11225	72	89	8937.5	11187.5
39	7937	7071	8909	57	71	7062.5	8937.5
38	6299.6	5612	7071	45	56	5562.5	7062.5
37	5K	4454	5612	36	44	4437.5	5562.5
36	3968.5	3536	4454	29	35	3562.5	4437.5
35	3149.8	2806	3536	23	28	2812.5	3562.5
34	2.5K	2227	2806	18	22	2187.5	2812.5
33	1984	1768	2227	15	17	1812.5	2187.5
32	1575	1403	1768	12	14	1437.5	1812.5
Δf = 5 Hz Low Group		Filter Corner = 2 kHz		Fs = 5.12 kHz			
31	1250	1114	1403	224	287	1117.5	1437.5
30	992	884	1114	178	223	887.5	1117.5
29	787	702	884	141	177	702.5	887.5
28	625	557	702	112	140	557.5	702.5
27	496	442	557	89	111	442.5	557.5
26	394	351	442	71	88	352.5	442.5
25	312.5	278	351	56	70	277.5	352.5
24	248	221	278	45	55	222.5	277.5
23	197	175	221	36	44	177.5	222.5
22	156.25	139	175	28	35	137.5	177.5
21	124	110	139	23	27	112.5	137.5
20	98	88	110	18	22	87.5	112.5
19	78	69.6	88	15	17	72.5	87.5
18	62	55.2	69.6	12	14	57.5	72.5
17	49.2	43.8	55.2	9	11	42.5	57.5

Table 5-6. One-Third (1/1) Octave Bands (Continued)

1/3 Octave Analysis Range = 80 kHz

Band No.	Band Center Frequency (C.F.)	C.F. $\times 2^{-1/6}$	C.F. $\times 2^{1/6}$	Low Cell	High Cell	Low Frequency	High Frequency
Δf = 250 Hz High Group		Filter Corner = 100 kHz		Fs = 256 kHz			
49	80 kHz	71272	89797	286	359	71375	89875
48	63496	56569	71272	227	285	56625	71375
47	50397	44898	56569	180	226	44875	56625
46	40K	35636	44898	143	179	35625	44875
45	31748	28284	35636	114	142	28375	35625
44	25198	22449	28284	90	113	22375	28375
43	20K	17818	22449	72	89	17875	22375
42	15874	14142	17818	57	71	14125	17875
41	12599	11225	14142	45	56	11125	14125
40	10K	8909	11225	36	44	8875	11125
39	7937	7071	8909	29	35	7125	8875
38	6299.6	5612	7071	23	28	5625	7125
37	5K	4454	5612	18	22	4375	5625
36	3968.5	3536	4454	15	17	3625	4375
35	3149.8	2806	3536	12	14	2875	3625
Δf = 7.8125 Low Group		Filter Corner = 3 kHz		Fs = 8 kHz			
34	2.5K	2227	2806	286	359	2230.5	2808.6
33	1984	1768	2227	227	285	1769.5	2230.5
32	1575	1403	1768	180	226	1402.3	1769.5
31	1250	1114	1403	143	179	1113.3	1402.3
30	992	884	1114	114	142	886.7	1113.3
29	787	702	884	90	113	699.2	886.7
28	625	557	702	72	89	558.6	699.2
27	496	442	557	57	71	441.4	558.6
26	394	351	442	45	56	347.7	441.4
25	312.5	278	351	36	44	277.3	347.7
24	248	221	278	29	35	222.6	277.3
23	197	175	221	23	28	175.8	222.6
22	156.25	139	175	18	22	136.7	175.8
21	124	110	139	15	17	113.3	136.7
20	98	88	110	12	14	89.8	113.3

Table 5-7. Analysis Range Coding

Range	Range Code (Bits)					
	5	4	3	2	1 (LSB)	
1 Hz	0	0	0	0	0	
2	0	0	0	0	1	
4	0	0	0	1	0	
5	0	0	0	1	1	
10	0	0	1	0	0	
20	0	0	1	0	1	
40	0	0	1	1	0	
50	0	0	1	1	1	
100	0	1	0	0	0	
200	0	1	0	0	1	
400	0	1	0	1	0	
500	0	1	0	1	1	Narrowband
1 kHz	0	1	1	0	0	
2	0	1	1	0	1	
4	0	1	1	1	0	
5	0	1	1	1	1	
10	1	0	0	0	0	
20	1	0	0	0	1	
40	1	0	0	1	0	
50	1	0	0	1	1	
100	1	0	1	0	0	
2 kHz	1	1	1	0	1	
4	1	1	1	1	0	
5	1	1	1	1	1	
10	1	1	0	0	0	1/3 Octave
20	1	1	0	0	1	
50	1	1	0	1	1	
100	1	1	1	0	0	

The DUAL and UPPER signal sources are located on the Front-Panel Interface Assembly (A5A18) at U16 (see drawing no. 2149700). The Motherboard (A1A1) accommodations have been made to include the required interconnection of the A5A18, A5A7, A5A1 and A5A2 circuit boards.

5.2.4.2 Logic Controller

The Logic Controller (as described in Section 2) provides micro-instructions for all tasks required to process the digitized outputs of the Signal Conditioners to Input Memory. The Logic Controller has been reprogrammed to include the subroutines required to process one-third octave data. The detailed circuit description in Section 2 of this manual contains an Input Memory Control Logical Flow Diagram (Figure 2-15) which includes 1/3 octave subroutines at 87 and 91.

5.2.5 Timing and Control

The Timing and Control Assembly (A5A6) used by the SD375-2 Option generates two sampling frequencies instead of one as with the basic instrument. The fundamental 16.384 MHz oscillator output is divided and multiplexed to provide the 28 different signals required by the Input Signal Conditioners. All 1/3 octave sample frequencies are internally generated. If an external sampling frequency is selected, one-third octave is disabled by A5A6U29.

Figure 5-8 is a simplified block diagram of one-third octave timing circuitry. Only one of the two available outputs is used by either input Signal Conditioner A or B. The divide-by-25 outputs from U58 is selected by U48 and used by A5A1 (Signal Conditioner A) for high group A/D conversion. The divide-by-32 output from U57 is selected and used by A5A2 for low group A/D conversion.

5.2.6 Memory Hardware/Software Changes

5.2.6.1 Micro-Program Control

The additional machine software instructions required by the one-third octave option were generated to (1) process the input memory data through the 3000 CPE, (2) control the timing of numerous operations, and (3) control the busing of data. The 1/3 octave version of the Micro-Program Control Assembly (A5A11) incorporates a different memory configuration using *30*K of memory vice the standard 28K memory array. The 1/3 octave version of A5A11 uses an AM27PS191DC (2K $\times$ 8) instead of the 82S181 (1K $\times$ 8) PROMs.

5.2.6.2 Control Processor

The Z80 Instruction PROMs (A5A8U83-88) were modified to include 1/3 octave instructions needed to transfer 1/3 octave data to and from the 3000 CPE.

5.2.6.3 Memory Address

The Memory Address Assembly (A5A15) incorporates a different ROM set programmed to provide a set of coefficients used by the Arithmetic Processor for 1/3 octave computations.

5.2.6.4 Video Interface

The video Interface Assembly (A5A16) incorporates a different version of the "X-Line" PROM (A5A16U91). This new PROM provides the 1/3 octave grids on the raster scan crt.

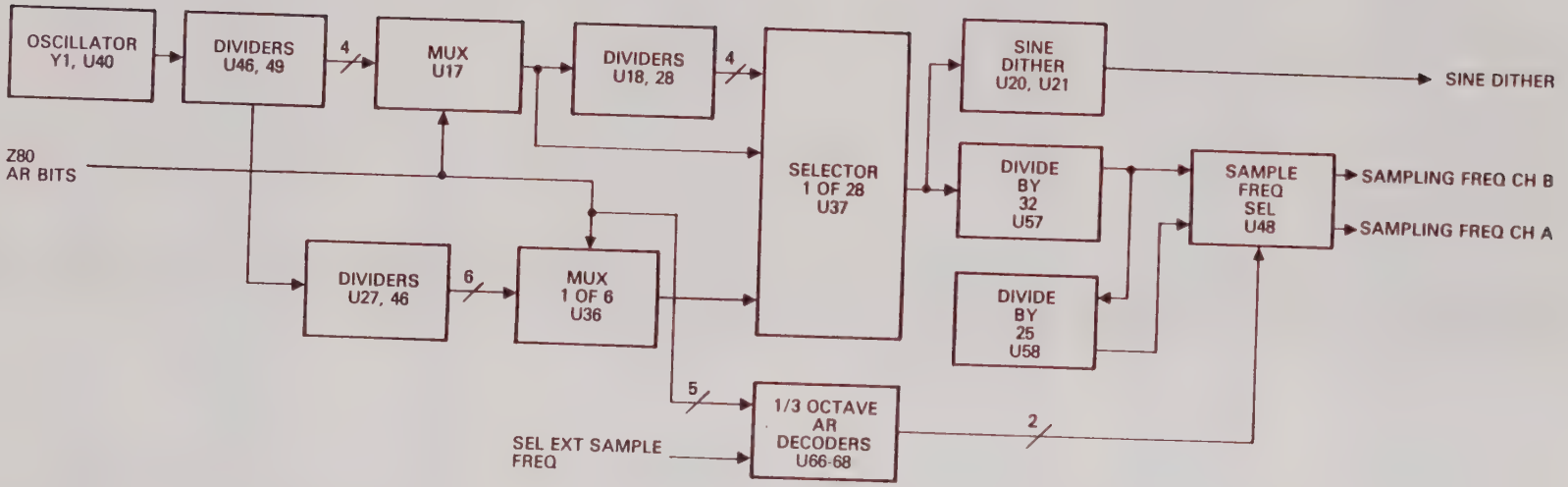


Figure 5-8. One-Third Octave Timing Circuitry

5.2.6.5 Motherboard

The following list summarizes Motherboard (A1A1) Assembly Interconnections required (in units serial-numbered below 216) to retrofit the SD375 for "-2" option operation.

3000 D Bus 2[1]	A7-85A, A18-128
STAT 5	A8-89A, A17-88A
SEL SD346	A7-89A, A8-87A
	A20-44, A6-32A
A to Both	A7-26B, A2-16A, A11-21A
B to Both	A7-28B, A1-16A
UPPER	A7-24B, A18-54
DUAL	A7-22B, A18-56
Third Octave	A7-12B, A6-86A
Sample Frequency A	A6-94A, A1-94A
Sample Frequency B	A6-90A, A2-94A
AR 100 kHz to A1	A6-60B, A1-34B
AR 100 kHz to A2	A6-34B, A2-34B
Normalized Sig. 2	A1-86A, A2-85A
Normalized Sig. 1	A1-85A, A2-86A
Gnd B	A1-31B, A1-71B

The following connections have been eliminated on "-2" option Motherboard Assemblies serial numbered below 216.

EXECUTE	A7-98A, A6-90A
Sample Freq (FS)	A2-94A, A1-94A (Side 1)
	A2-94A, A3-94A (Side 1)
AR100 kHz	A2-34B, A1-34B (Side 1)
	A2-34B, A3-34B (Side 1)
	A6-34B, A5-34B (Side 1)
AR16 String	A1-31B, A2-31B (Side 1)

5.3 DIGITAL I/O INTERFACE ASSEMBLY

5.3.1 I/O Interface (-3 Option) General Description

The -3XXX I/O option is a single card which, when installed in the SD375 DYNAMIC ANALYZER II, provides the instrument with digital interfacing capability across two ports:

IEEE standard 488 — "Digital interface for programmable instrumentation"

EIA standard RS-232-C — "Interface between data terminal equipment and data communication equipment employing serial binary data interchange"

The RS-232-C interface is a *serial* binary interface in use throughout the computer industry, and is found on a large number of computers and peripherals. It is the interface normally implemented on modems (devices used to enable data communication over telephone lines). RS-232-C configurations normally have only two devices in communication on any one interface. A device with a need to communicate with more than one other device would have to have more than one RS-232-C interface.

The IEEE interface is a parallel 8 (data) bit "bus". The IEEE standard electrically defines bi-directional, tri-state lines and a device addressing protocol which allows up to 15 devices to be connected to a single interface bus. One device would be a "controller", which directs data communication on the bus. Configurations without a controller require that only one device be enabled to talk. All remaining devices must be enabled only to listen. These are the talk-only and listen-only functions of the IEEE interface.

The I/O can be set up to respond to control from either the IEEE or the RS-232-C interface. Regardless of whichever port has been assigned control, the other port is still active, and data communications over that port can be initiated from either the controlling port or the front panel.

Full front panel controls are provided which allow the user to review his I/O setup, modify it, select a data type and interface to transfer, and execute such a transfer. This gives the user the ability to exercise I/O control when there is no computer in the system, or to override the settings of the I/O card switches.

When under the control of a computer, the I/O gives that computer the ability to lock out the front panel of the SD375, operate all front panel keys, define configurations for the instrument to assume, read status and configuration information out, read signal processing results in several formats, enter signal information in various formats for post-processing, write messages on the SD375's CRT, and direct the SD375 to generate an interrupt upon the occurrence of some event.

5.3.2 Digital I/O System Overall Concept

The Digital I/O System Option circuitry is located on the A5A9 printed wiring assembly. Figure 5-9 is an overall block diagram of the I/O Option operation.

The Z80 Microprocessor, which controls interface between the 3000 Microprocessor, front-panel touch controls, and the CRT of the SD375 also controls data transfer and port selection on the I/O Option circuitry.

The three areas of functional control exercised by the Z80 microprocessor over I/O interface operations are summarized in the following paragraphs.

Z80 I/O Port Control

The Z80:

Reads the I/O option card DIP (dual in-line packaged) switches.

Writes on the LED latches.

Reads or writes on the IEEE or the RS-232-C as I/O ports.

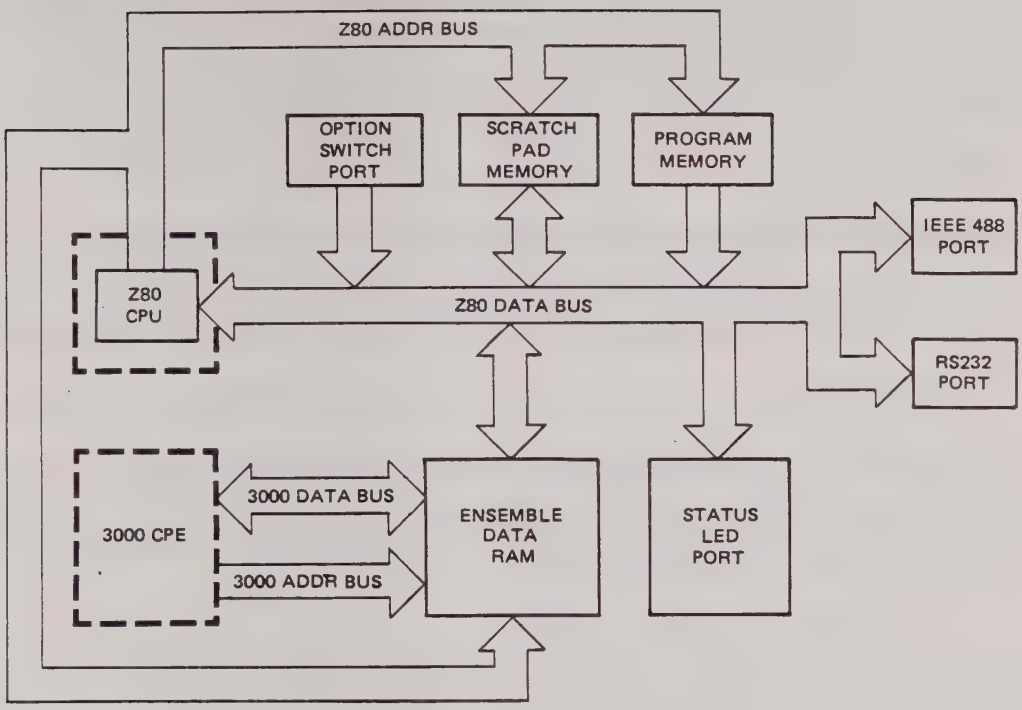


Figure 5-9. I/O Interface (-3 Option) Overall Block Diagram

I/O Port Hardware External Interface

The IEEE 488 port:

Interfaces the Z80 to an external IEEE bus.

The RS-232-C port:

Interfaces the Z80 to an external bus.

Z80 Ensemble Data Memory Control

The Z80:

Reads from/Writes to the Ensemble Data MEMORY which is also accessible to the 3000 Microprocessor.

Reads from/Writes to the SCRATCH PAD MEMORY for I/O Z80 flags and registers.

Reads the Program Memory for I/O Z80 firmware.

These three main areas of Z80 control functions and the I/O interrupt structure are explained in further detail in subsequent paragraphs. The functional block diagram (Figure 5-10) and the A5A9 schematics (drawing number 21255100 sheets 1 through 7) should be used in conjunction with the following descriptive information.

5.3.3 Z80 I/O Port Control

There are three primary input/output parts addressed on the I/O Interface Assembly. These are:

a. The I/O Status LEDs which are fed by Status Latch (U40) and Drivers (U25 and U26), the Protocol Switch (U12), the Data Control Switch (U13), and/or the RS-232-C Switch (U14).

b. The IEEE 488 compatible General Purpose Interface Bus (GPIB) Talker Listener (U64).

c. The RS-232-C compatible Programmable Communications Interface (U1).

Port selection is accomplished by U20 (Port Address Decoder) which decodes the Buffered Z80 Address Bus bits A3 - A5 to select one of the three ports listed above.

Buffered Z80 Address Bus bits A0 - A2 are decoded by the I/O Address Decoder (U44) to select the I/O Status LEDs, the Protocol Switches, the Data Control Switch, or the RS-232-C Switch when Port Address Decoder (U20) signals *I/O Decode*.

The Function Set and I/O Card Protocol Switches (U12, U31), the Data Control Switch, and the I/O card RS-232-C Switch are read during *power-up* or LOGO initialization.

The I/O Address Decoder (U44) outputs, Z80 MEM READ and B Read I/O (the two signals originate at the Control Processor), are fed to Switch Driver Select Logic (U46, 74, 75, and 76) to select the Protocol (U27), Data Control (U28), or the RS-232-C (U29) Switch Driver outputs on the Buffered I/O Data Bus. These two control signals enable the I/O Control Ports to be read by the Z80 microprocessor.

The Z80 MEM Write from the Control Processor (A5A8) and OL2 from the I/O Address Decoder (U44) check the I/O Status Latch to drive the Status LEDs (U10 and U11) through drivers (U25 and U26).

The Z80 MEM WRITE signal from the Control Processor Z80 Control Logic to the Asynchronous Communications Element (ACE) U1 *DOSTR* input and to the GPIB (U64) WR input allows the Z80 microprocessor to write data to the internal register selected by Buffered Z80 Address Bus Bits (A0 → A2) or either device.

To read data from either the ACE (U64) or the GPIB (U1), the Port Address Decoder (U20) is decoded as I/O RS-232-C or I/O IEEE, respectively. These two signals are fed to RS-232-C Select Logic (U4, U45, U61) or IEEE Select Logic (U46, U61, U77), respectively.

Chip select inputs to the ACE or the GPIB are thereby developed. The *DISTR* input to the ACE (U64) or the RD input to the GPIB enable the reading of internal ACE or GPIB data register data (by the Z80 microprocessor) as determined by bits A0 → A2 on the Buffered Z80 Data Bus.

5.3.4 I/O Port Hardware External Interface (IEEE)

The external interface lines on the GPIB (U64) are divided into three groups. These are Bus Control, Handshake and Data lines. The following paragraphs describe the Bus Control and Handshake lines. The data lines (D101 through D108) are the data transfer lines between the GPIB (U64) and an external device. (Refer to schematic drawing 21255100 Sheets 5 and 6.)

All 16 external interface lines are operated through general purpose interface bus transceivers (U63 for bus control and handshake bits while U78 handles input/output data bits).

5.3.4.1 Bus Control

EOI (End or Identify)

This signal can be sent by the I/O Option or an external control device. IEEE SEL LOGIC and the *Z80 MEM WRITE* signal controls the receive (listener) or transmit (talker) status of the line. EOI is normally high during transfer of data and set low by the talking device as the last data byte is transferred.

SRQ (Service Request)

This signal is available to indicate that the GPIB (U64) chip is ready to provide information (from a previous request) and needs an attention (ATN) control signal to start. Request for service will be indicated by the line going low.

REN (Remote Enable)

This signal is received by the GPIB from an external control device and selects (in conjunction with other messages) remote or local control of the SD375. With no input connection the line is high.

IFC (Interface Clear)

This signal is received by the GPIB (U64) from an external control device. With no input connection, the line is high. With a low input, the IEEE chip interrupts the in-process operation and will restart at the beginning when data transfer is restarted from the external device.

ATN (Attention)

This signal is received by the GPIB (U64) from an external control device. The line is set low by the external control device to indicate that the data being transferred on the data lines (DIO) by the external device is command or addressing information (first byte is primary address, second byte is secondary address).

5.3.4.2 Handshake

To transfer data between the GPIB (U64) and an external device, a synchronizing process must be accomplished between the two units. This handshake process insures that only valid data is transferred between any number of sources or acceptors. The three handshake signals are as follows:

NDAC (Not Data Accepted)

This signal line can be set to a high or low level by the I/O Option or an external control device. The IEEE RD/WR logic controls the talk or listen status of the line. The line is a controlling element in the handshake process to indicate the condition of data acceptance by the GPIB (U64) or the external control device.

NRFD (Not Ready for Data)

This signal line can be set to a high or low level by the I/O Option or an external control device. The IEEE RD/WR logic controls the talk or listen status of the line. The line is a controlling element in the handshake process to indicate the readiness of the GPIB (U64) or an external device to transfer data.

DAV (Data Valid)

This signal line can be set to a high or low level by the I/O Option or an external control device. The IEEE RD/WR logic controls the talk or listen status of the line. The line is a controlling element in the handshake process to indicate to a listener that information on the data lines (DIO) from a talker is available and valid for transfer.

5.3.5 I/O Port Hardware External Interface (RS-232-C)

The RS-232-C chip, though not defined as a handshake synchronous interface device, can be made to approximate a handshake by using the modem control lines. Some devices never use these lines or do not use them in a manner compatible with the I/O Option. It is entirely possible, however, to simply not hook up the control lines and operate the RS-232-C portion of the I/O Option entirely on the transmit and receive lines.

5.3.5.1 Output Lines

There are nine lines connected to the rear-panel RS-232-C connector (J21) three Line Drivers (U32, 33, 47, 48). Four (4) of the lines are signal outputs while the remaining lines are signal inputs. The effective outputs are described below.

DTR (Data Terminal Ready)

When low, informs the MODEM or data set that the RS-232-C port is ready to communicate. The DTR output signal is set to an active low. The DTR signal is set high upon a Master Reset operation.

RTS (Request to Send)

When low, informs the MODEM or data set that the RS-232-C port is ready to transmit data. The RTS output signal is set to an active low. The RTS signal is set high upon a Master Reset operation.

SOUT (Transmitted Data)

Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the logic 1 state upon a Master Reset operation.

5.3.5.2 Input Lines

The input lines on the RS-232-C connector which are active are as follows:

CTS (Clear to Send)

The CTS signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 of the MODEM Status Register. Bit 0 of the MODEM Status Register indicates whether the CTS input has changed state since the previous reading of the MODEM Status Register. Whenever bit 4 of the MODEM Status Register changes state, an interrupt is generated.

SIN (Received Data)

Serial data input from the communications link (peripheal device, MODEM or data set).

5.3.6 Z80 I/O Interface Memory Control

The Control Processor Assembly exercises control over the Ensemble Data Memory via the I/O Interface Memory Control Logic (U5, 6, 7, 8, 21, 23, 24 and 38), the Ensemble Data Memory Selector (U22), the Ensemble Memory Address Selector (U49, U65, U79), and the Buffered Address Bus or the 3000 Address Bus.

Data is received from/sent to the 3000 CPE under control of I/O Interface Memory Control Logic via 3000 Data Bus Drivers (U80-U83).

5.3.6.1 Ensemble Memory Data Read/Write Operation

The 3000 TRANS C EN (3000 TRANSFER CHIP ENABLE) signal from the I/O Status Latch (U40) is part of the I/O Interface Memory Control Logic, Ensemble Memory Address Selector enable, Ensemble Memory Chip Select Logic, and the Ensemble Memory Bus Driver Select Logic.

When 3000 TRANS C EN is high:

The 3000 Address Bus input to the Ensemble Memory Address Selector (U49, 65, 79) is selected for transfer to the Ensemble Data Memory via the Ensemble Memory Address Bus.

The B inputs to the Ensemble Memory Chip Selector (U22) are selected to enable the A or B section of the Ensemble Data memory for the read operation.

The EVEN 1 and EVEN 2 signals are both low to place Ensemble Memory Data on the Buffered I/O Data Bus via the Ensemble Memory Buffers.

When 3000 TRANS C EN is low:

The Buffered Z80 Address Bus is selected via the Ensemble Memory Address Selector (U49, 65, 79) and the Memory Address Bus.

The A inputs to the Ensemble Memory Chip Selector (U22) enable the A or B section of the Ensemble Data Memory for the write operation.

The EVEN 1 and EVEN 2 signals are high to allow data on the Buffered I/O Data Bus to the Buffered 3000 Data Bus via the Ensemble Memory Buffers.

5.3.6.2 Program Memory

The Program Memory (U70-73 on sheet 4 of drawing 21255100) is addressed by the Z80 via the Buffered Z80 Address Bus. Bit A11 is the output enable (OE) input while bit A12, I/O PROM EN 1 and I/O PROM EN 2 are decoded by the Program Memory Chip Select Logic (U59, U76) to select the appropriate 1K block to be addressed.

Program Memory Driver (U54) is gated on by PROM/SCRATCH PAD Select Logic (U4, 45, 75, 76, 77) inputs (PROM 1 or 2, B READ I/O, and Z80 MEM READ).

5.3.6.3 Scratch Pad RAM

The Scratch Pad (U55-58) is a 2K byte Random Access Memory used to read or write Z80 register data and flags.

It is addressed by the Z80 address on the Buffered Z80 Address Bus and selected by Scratch Pad Chip Select Logic (U45, 76) inputs (I/O RAM 2 and Z80 Address Bit A10). The write enable signal is Z80 MEM WRITE from the Control Processor.

The *Z80 Memory Write* signal enables the Scratch Pad Input Drivers (U39-2, U41-2) during the write operation.

The Scratch Pad Output Drivers (U39-1, U41-1) are enabled by I/O RAM 2, Z80 MEM READ, and B READ I/O signals to the PROM/Scratch Pad Select Logic (U4, U76).

5.3.7 I/O Interrupts

The I/O Interrupts are generated by the GPIB (U64) or the ACE (U1) and are controlled by the Z80 Interrupt Mode 2.

5.3.7.1 Interrupt Mode 2

When the Z80 receives an interrupt from the I/O Interface Assembly at its INTERRUPT input, it accesses the hexidecimal code (C1) from its internal I Register. This code forms the MSBs of the address in the Control Processor Instruction PROMs of the service routine for the Interrupt being processed. The Z80 CPU acknowledges the interrupt with I/O INTERRUPT ACK to Inverter U74 (drawing 21255100 sheet 5), reads the 8-bit Interrupt Vector from the Interrupt Priority Latch (U42) as the two Hexidecimal LSBs of the address in memory of the service routine for the I/O Interface.

5.3.7.2 I/O Interrupt Vector Generation

The INTRPT output from the ACE (RS-232-C) and the INT output from the GPIB (IEEE 488) are fed to Interrupt Priority Encoder (U43).

If both interrupts were present at the same time, the GPIB (U64) interrupt would take precedence.

A three (3) bit output (000 for GPIB-IEEE or 001 for ACE-RS-232-C interrupts) is generated by the Interrupt Priority Encoder (U43) along with GS which signals the Z80 CPU of the Interrupt by switching the State of Flip Flop U30 when M1C goes low. U30-Q also clocks the Interrupt Priority Latch (U42) to load the three bits (A0 → A2) from U43 and the five hard-wired bits.

The Interrupt Priority Latch places the 8-bit vector on the Buffered I/O Data Bus when I/O Interrupt Ack is received from Z80 Control Logic via the Interrupt Priority Logic (U46). The vector is simultaneously placed on the Z80 Data Bus by INT EN BUS from U46 which enables Z80 Data Bus Drivers (U86-U89).

There are two address vectors generated by the Interrupt Priority Latch. The GPIB (IEEE-488) interrupt vector is 10 (Hex). The ACE (RS-232-C) interrupt vector is 12 (Hex). When added to the Z80-CPU I Register Contents, the addresses become C110 (Hex) and C112 (Hex), respectively.

The Z80 then reads the appropriate I/O interrupt service program address out of RAM location C110 or C112 and jumps to it (after "pushing" the current program count onto the stack — an internal Z80 function). These address locations in RAM will contain the program addresses of the RS-232-C and IEEE 488 routines as stored during initialization.

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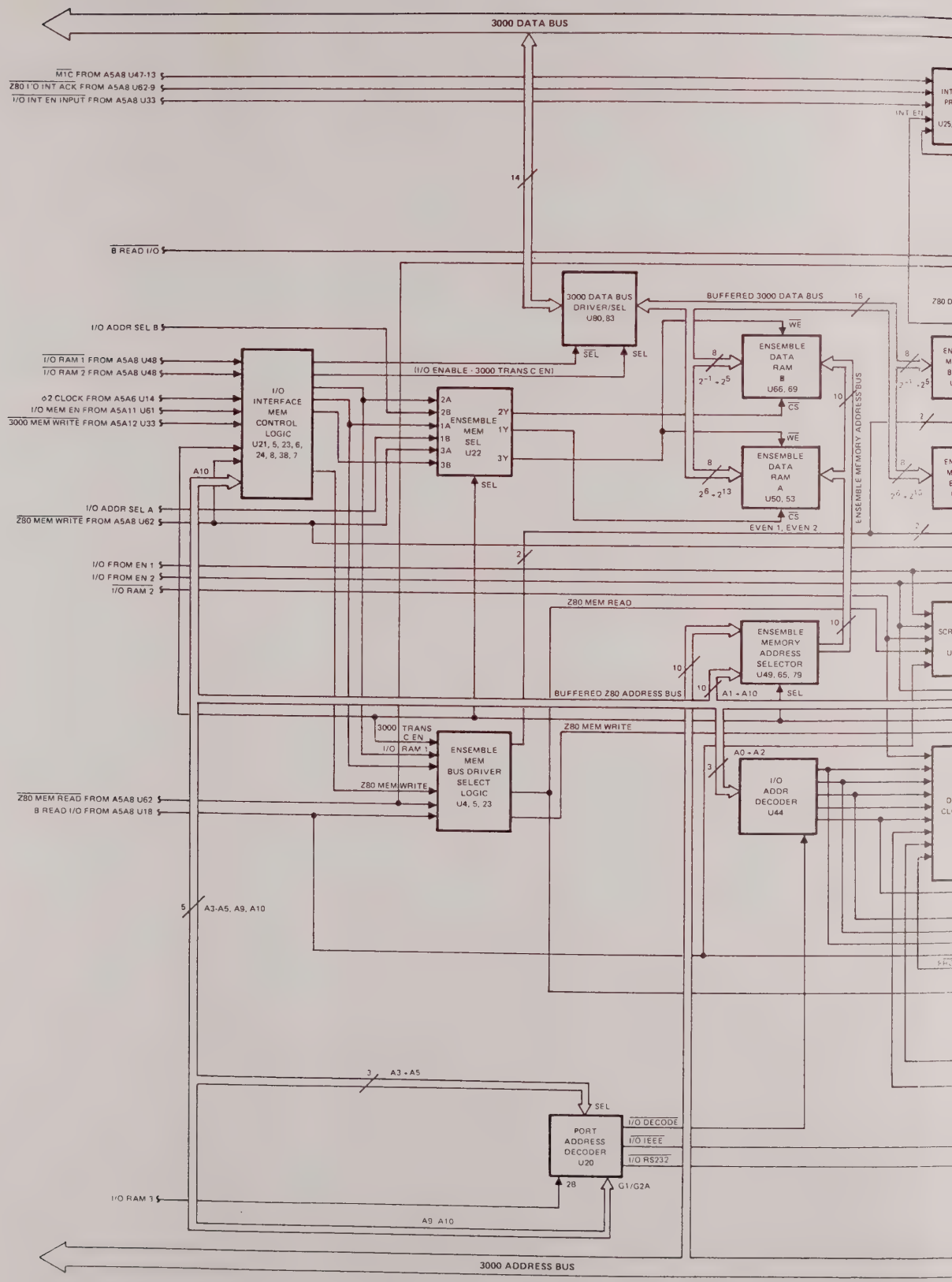
3000 DATA BUS
M1C FROM A5A8 U47-13
Z80 I/O INT ACK FROM A5A8 U62-9
I/O INT EN INPUT FROM A5A8 U33
14
8 READ I/O
3000 DATA BUS DRIVER/SEL U80, 83
BUFFERED 3000 DATA BUS
16
I/O ADDR SEL B
I/O RAM 1 FROM A5A8 U48
I/O RAM 2 FROM A5A8 U48
I/O ENABLE · 3000 TRANS C EN
SEL
WE
ENSEMBLE DATA RAM B U66, 69
CS
ENSEMBLE DATA RAM A U50, 53
EVEN 1, EVEN 2
ENSEMBLE MEMORY ADDRESS BUS
ϕ2 CLOCK FROM A5A6 U14
I/O MEM EN FROM A5A11 U61
3000 MEM WRITE FROM A5A12 U33
I/O INTERFACE MEM CONTROL LOGIC U21, 5, 23, 6, 24, 8, 38, 7
A10
ENSEMBLE MEM SEL U22
2A
2B
1A
1B
3A
3B
2Y
1Y
3Y
I/O ADDR SEL A
Z80 MEM WRITE FROM A5A8 U62
I/O FROM EN 1
I/O FROM EN 2
I/O RAM 2
Z80 MEM READ
ENSEMBLE MEMORY ADDRESS SELECTOR U49, 65, 79
BUFFERED Z80 ADDRESS BUS
A1 - A10
3000 TRANS C EN
I/O RAM 1
Z80 MEM WRITE
ENSEMBLE MEM BUS DRIVER SELECT LOGIC U4, 5, 23
A0 - A2
I/O ADDR DECODER U44
Z80 MEM READ FROM A5A8 U62
8 READ I/O FROM A5A8 U18
A3-A5, A9, A10
A3 - A5
PORT ADDRESS DECODER U20
I/O DECODE
I/O IEEE
I/O RS232
2B
G1/G2A
I/O RAM 3
A9, A10
3000 ADDRESS BUS

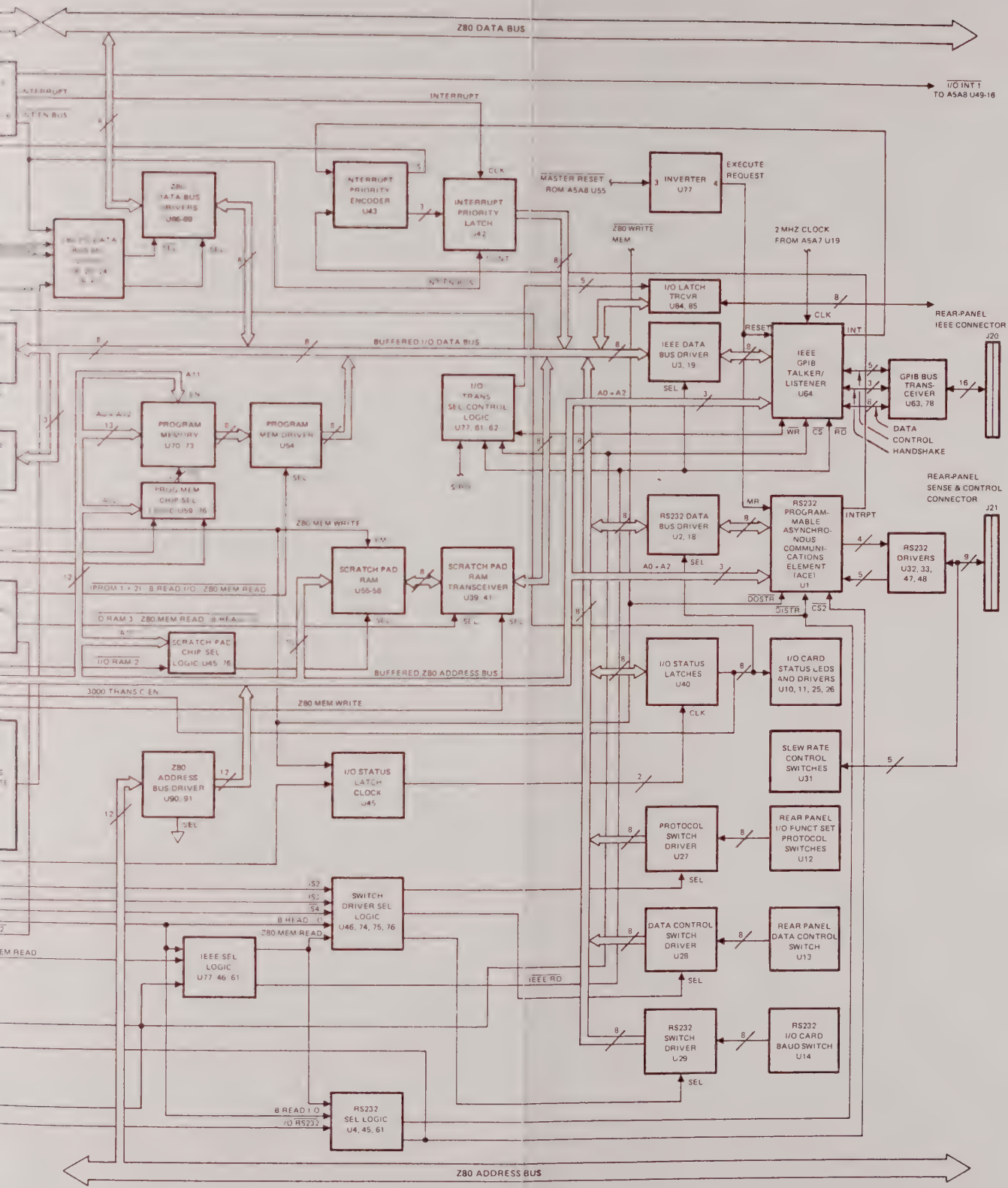
Z80 DATA BUS
I/O INT 1
TO A5A8 U49-16
INTERRUPT
INTERRUPT PRIORITY ENCODER U43
INTERRUPT PRIORITY LATCH U42
MASTER RESET
ROM A5A8 U55
INVERTER U77
EXECUTE REQUEST
Z80 WRITE MEM
2 MHZ CLOCK FROM A5A7 U19
I/O LATCH TRCVR U84, 85
REAR-PANEL IEEE CONNECTOR
J20
BUFFERED I/O DATA BUS
IEEE DATA BUS DRIVER U3, 19
IEEE GPIB TALKER/ LISTENER U64
GPIB BUS TRANS-CEIVER U63, 78
DATA CONTROL HANDSHAKE
I/O TRANS SEL CONTROL LOGIC U77, 61, 62
PROGRAM MEMORY U70 73
PROGRAM MEM DRIVER U54
PROG MEM CHIP SEL
Z80 MEM WRITE
SCRATCH PAD RAM U55-58
SCRATCH PAD RAM TRANSCEIVER U39 41
SCRATCH PAD CHIP SEL LOGIC U45 76
BUFFERED Z80 ADDRESS BUS
RS232 DATA BUS DRIVER U2, 18
RS232 PROGRAM-MABLE ASYNCHRO-NOUS COMMUNI-CATIONS ELEMENT (ACE) U1
REAR-PANEL SENSE & CONTROL CONNECTOR
J21
RS232 DRIVERS U32, 33, 47, 48
I/O STATUS LATCHES U40
I/O CARD STATUS LEDS AND DRIVERS U10, 11, 25, 26
SLEW RATE CONTROL SWITCHES U31
Z80 ADDRESS BUS DRIVER U90, 91
I/O STATUS LATCH CLOCK U45
PROTOCOL SWITCH DRIVER U27
REAR PANEL I/O FUNCT SET PROTOCOL SWITCHES U12
SWITCH DRIVER SEL LOGIC U46, 74, 75, 76
DATA CONTROL SWITCH DRIVER U28
REAR PANEL DATA CONTROL SWITCH U13
IEEE SEL LOGIC U77 46 61
IEEE RD
RS232 SWITCH DRIVER U29
RS232 I/O CARD BAUD SWITCH U14
RS232 SEL LOGIC U4, 45, 61
Z80 ADDRESS BUS

Figure 5-10. I/O Interface Assembly (A5A9) Functional Block Diagram

5.4 SYNCHRONOUS SIGNAL GENERATOR (-4 OPTION)

5.4.1 General Description

The "-4 option" of the SD375 Dynamic Analyzer II is a convenient source of broadband white noise, band limited pseudo-random noise, and single sinewave analog outputs for the excitation of external systems or networks for performance evaluation. The signal generator output mode is established from a program (PRGM) menu and its outputs amplitude is selectable from 0.05V to 5V in a 1, 2, 5 sequence.

The pseudo-random noise is synchronized to the analog-to-digital (A/D) converter clock supplied by/generated by timing and control circuitry on the A5A6 assembly. The Synchronous Signal Generator (SSG) produces a sequence length which matches the memory period of the analyzer. A trigger output, coincident with the start of each sequence is provided. In the zoom modes, the pseudo-random frequency output is concentrated within the selected zoom window.

Figure 5-11 is an overall block diagram of SSG operation illustrating the circuit signal paths for broadband white noise, band-limited pseudo-random noise, and single sinewave analog generation.

Figure 5-11 also identifies the hardware devices composing each major circuit element. These major circuit elements are described in the circuit analysis which follows.

5.4.1.1 Broadband Noise Circuit Analysis

The Broadband Noise Source is zener diode CR5. Thermal noise produced is amplified by U5 and U6.

When selected, the amplified random noise is fed through K6 (pins 14 and 7/8) to the Gain Controlled Output Amplifier (U12 and U13).

The broadband noise from U12 and U13 is available at J17 on the Rear Panel Assembly for external EXCITATION.

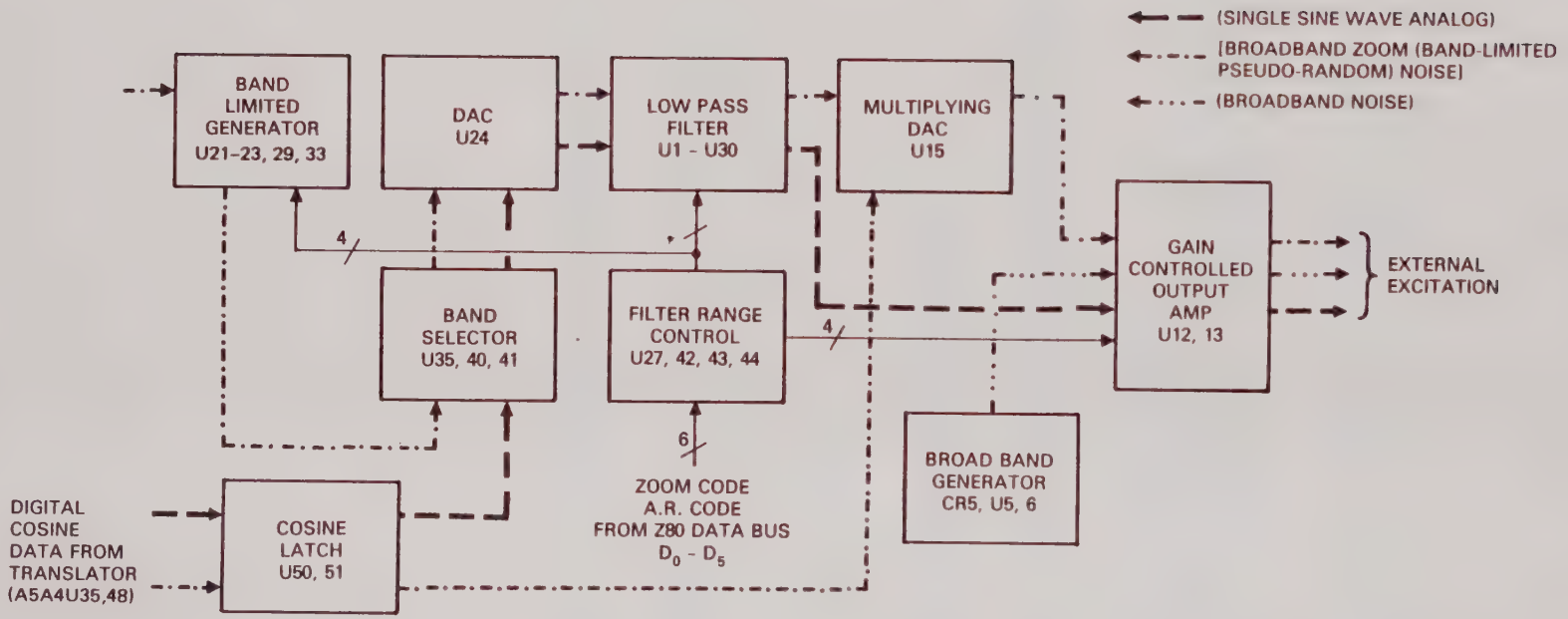
(SINGLE SINE WAVE ANALOG)
(BROADBAND ZOOM (BAND-LIMITED PSEUDO-RANDOM) NOISE)
(BROADBAND NOISE)
BAND LIMITED GENERATOR U21-23, 29, 33
DAC U24
LOW PASS FILTER U1 - U30
MULTIPLYING DAC U15
GAIN CONTROLLED OUTPUT AMP U12, 13
EXTERNAL EXCITATION
BAND SELECTOR U35, 40, 41
FILTER RANGE CONTROL U27, 42, 43, 44
BROAD BAND GENERATOR CR5, U5, 6
DIGITAL COSINE DATA FROM TRANSLATOR (A5A4U35,48)
COSINE LATCH U50, 51
ZOOM CODE A.R. CODE FROM Z80 DATA BUS D_0 - D_5
4
4
6

Figure 5-11. SD375 Dynamic Analyzer II (-4 Option) Synchronous Signal Generator (SSG) Circuit Overall Block Diagram

5.4.2 Broadband Zoom and Narrowband (Single Frequency) Circuit Analysis

The following analysis includes a detailed discussion of both broad and narrowband generators of the SSG assembly. The detailed circuitry contained in the schematic drawing has been simplified in the block diagram of Figure 5-12 [Broadband Zoom (Band-Limited/Pseudo-Random) and Narrowband (single frequency) Circuitry].

5.4.2.1 Broadband Zoom

Timing and Control signals required to generate the broadband and narrowband excitation are brought into the Control Drivers (U48). These inputs include AR CLK (*Analysis Range Clock* from Timing and Control (A5A6)), LD STATUS from the Translator (A5A4), one of 21 selectable sampling frequencies (fs) depending on the selected analysis range, and the translator on (XLTR ON) signal.

The sample frequency (fs) is fed to the zoom counters (U29, 32, 47) where the six different zoom frequencies (zoom factors 2, 5, 10, 20, 50, 100) are computed and fed to the Zoom Counter Selector (U33). The latched zoom code (Z80 Data Bus bits D2–D4) are fed to select inputs ABC to select the appropriate frequency to the Address Counter (U21, 29).

The Address Counter counts from 0 to 1023 to strobe the Digital Pseudo-Random Noise Generator SSG #1 and SSG #2 (PROMs U22, U23), and produce the appropriate set of bits as the Address Counter is incremented.

The Digital Pseudo-Random Noise outputs from SSG #1 and 2 are programmed to generate the inverse Fourier transform. These outputs are latched by noise latch (U34, U36) with the output of the Zoom Counter Selector (U33) and feed out to Band Selector (U35, 40,41).

The MSB (2^9 bit) from the Address Counter triggers the Sync Pulse Generator (U20), a delay one-shot multivibrator, which produces the SYNC PULSE (reference) output of Control Driver (U48) when a complete ensemble (1024 samples) have been processed.

5.4.2.2 Narrowband (Single Frequency) Circuit Analysis

When the single frequency analog operation is selected the translator circuitry is required to provide the digital cosine data at the desired operating frequency. The cursor location establishes this frequency and results in the Translator (A5A4) Assembly supplying the required digital cosine data word to the SSG required to generate the analog output.

The Single Frequency signal (Z80 Data Bus bit D2) clears the XLTR Cosine Data Latch (U50, U51) via Narrowband Select Logic (U49).

The Band Selector enables its B inputs (XLTR COSINE DATA).

The Translator Clock (XLTR CLK) via U49 (Cosine Clock Logic) latches the Digital Cosine Data received from the Translator Assembly into U50 and U51). This digital cosine data (which is analogous of the selected frequency) is available at the Band Selector outputs on the single frequency (narrowband) mode of operation.

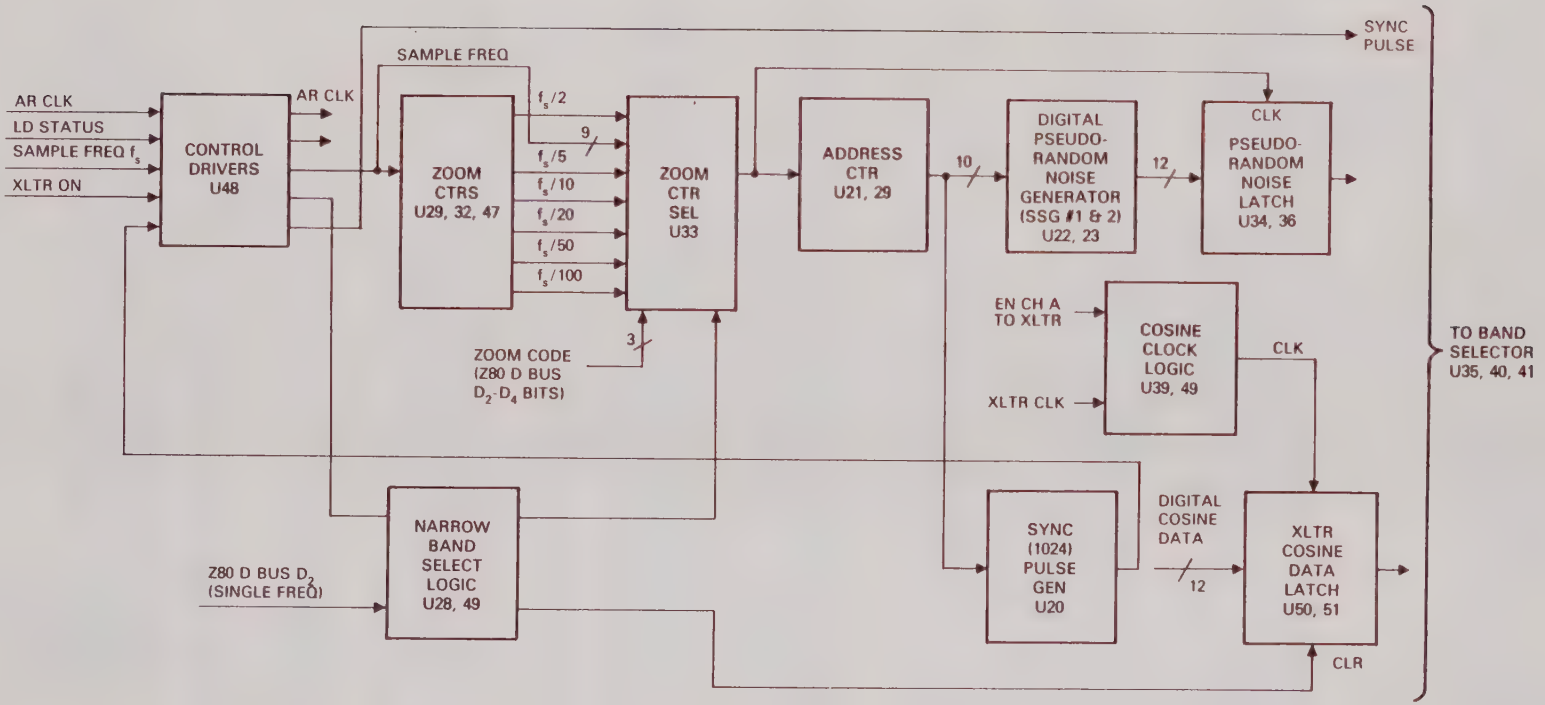

Figure 5-12. SSG Assembly (A5A17) Simplified Block Diagram — Broadband Zoom (Band-Limited/Pseudo-Random and Narrowband (Single Frequency) Circuitry

5.4.3 Band Selector

The Band Selector accepts 12 bits of digital cosine data from the Translator to the Digital-to-Analog Converter (DAC) U24 in Single Frequency operation as a result of the SINGLE FREQ bit at its select input being high. When the Single Frequency bit is low, the Band Limited Generator output is selected.

The Band Selector provides 1024 digital pseudo-random noise words to DAC (U24) when Broadband Zoom is selected.

5.4.4 Digital-to-Analog Converter (U24)

The DAC (U24) accepts the 12-bit digital inputs and produces a complimentary analog voltage at its output (pins 15, 18) which ranges from 0V to ± 5 VDC in steps of 4.88 mV per bit.

The DAC output is inverted by Amplifier U16 to compensate for internal DAC inversion.

5.4.5 Low Pass Filter (LPF)

The Low Pass Filter is composed of 11 Chopper Stabilized Operational Amplifiers and 4 (12-bit) multiplying DACs configured as a 4-pole elliptical filter.

The response of the LPF is controlled by switching the reactive components around amplifiers (U4, U8, U25, U30) via the Filter Range Control circuitry and relays K1 thru K4..

The Output (V_{OUT}) of each successive DAC/Amplifier pair is described by the formula:

$$V_{OUT} = V_{REF}\left(\frac{F_0}{2} + \frac{F_1}{4} + \frac{F_2}{8} + \ldots + \frac{F_{11}}{4096}\right)$$

where $F_n = 1$ if the digital input is high and $F_n = 0$ if the digital input is low.

The roll-off of the LPF at its output (TP11) is approximately 44 decibels per decade.

5.4.5.1 Voltage Regulation

The Low Pass Filter Assembly's chopper stabilized operational amplifiers receive their supply voltages (+5V and −5V) from 3-terminal IC Regulators U53 and U52 respectively.

5.4.5.2 Filter Range Control

The filter range control circuitry is illustrated in Figure 5-13 (Simplified Range Control Circuitry). This hardware accepts the range and zoom inputs from the Z80 Data Bus and (1) provides the 12-bit digitized filter corner frequency control signals to the Low Pass Filter DACs, (2) provides the Zoom Code to the Zoom Counter Selector (U33), and (3) decodes range and zoom inputs to control the configuration of reactive components which shape the LPF output.

5.4.6 Multiplying (M) DAC

The Multiplying DAC is only a functional circuit element when in the Broadband Zoom operating mode. It accepts the LPF output analog signal and the 12-bit latched Translator digital cosine data. (a function of the cursor location). The M-DAC operates in conjunction with the Chopper Stabilized Amplifiers U7 and U14 to produce the product of the digital cosine data fraction and the analog voltage at the V_{REF} input (LPF output).

The analog output voltage of the M-DAC appears at U14 pin 6 as:

$$V_{OUT} = -V_{REF}\left(\frac{E_1}{2} + \frac{E_2}{4} + \frac{E_3}{8} + \ldots + \frac{E_3}{2048}\right)$$

where $E_n = 1$ if the digital data cosine bit is high and $E_n = 0$ if the digital cosine data bit is low.

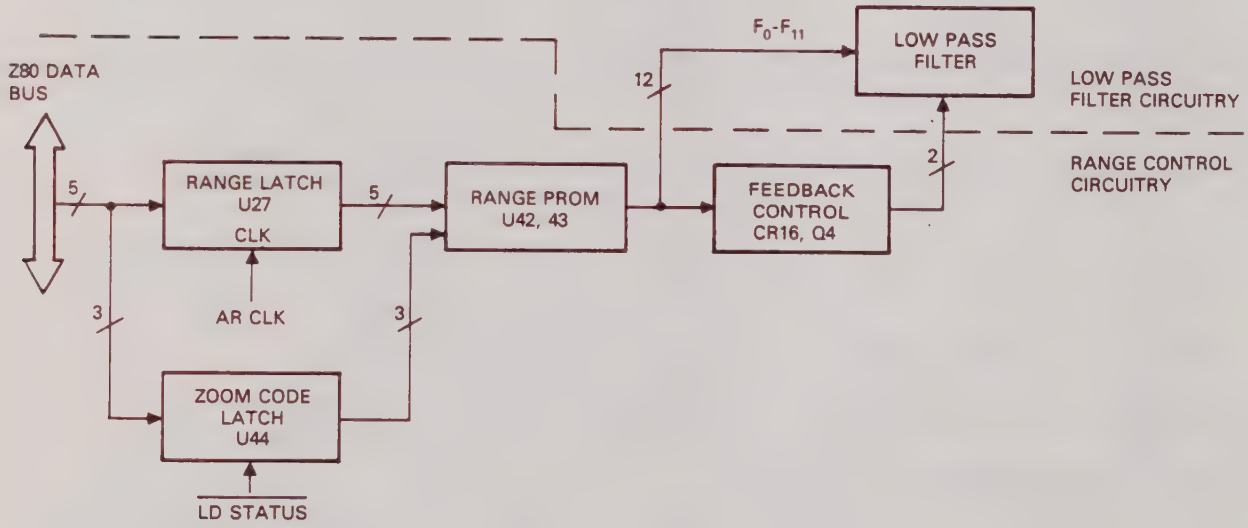

Figure 5-13. Simplified SSG Range Control Circuitry

The M-DAC output is a 1V normalized signal which is fed through the de-energized contacts of K5 (pins 7/8 and 1) in the broadband zoom mode of operation to the Gain Controlled Output Amplifiers.

5.4.7 Gain Controlled Output Amplifiers

The Gain Controlled Output Amplifiers scale the EXCITATION output at J17 on the rear-panel (in accordance with the front-panel gain selections) from the 1V normalized output of the M-DAC.

Figure 5-14 is a simplified functional block diagram of the Gain Controlled Output Amplifiers.

The Gain Code (Z80 Data Bus bits D3 → D5) is decoded by SSG #5 to select the input and feedback resistance network configuration on broadband amplifier U13. Buffered outputs are fed to appropriate relay drivers (Q5 through Q8) to set up the required gain or attenuation of the 1V normalized analog signal from the M-DAC.

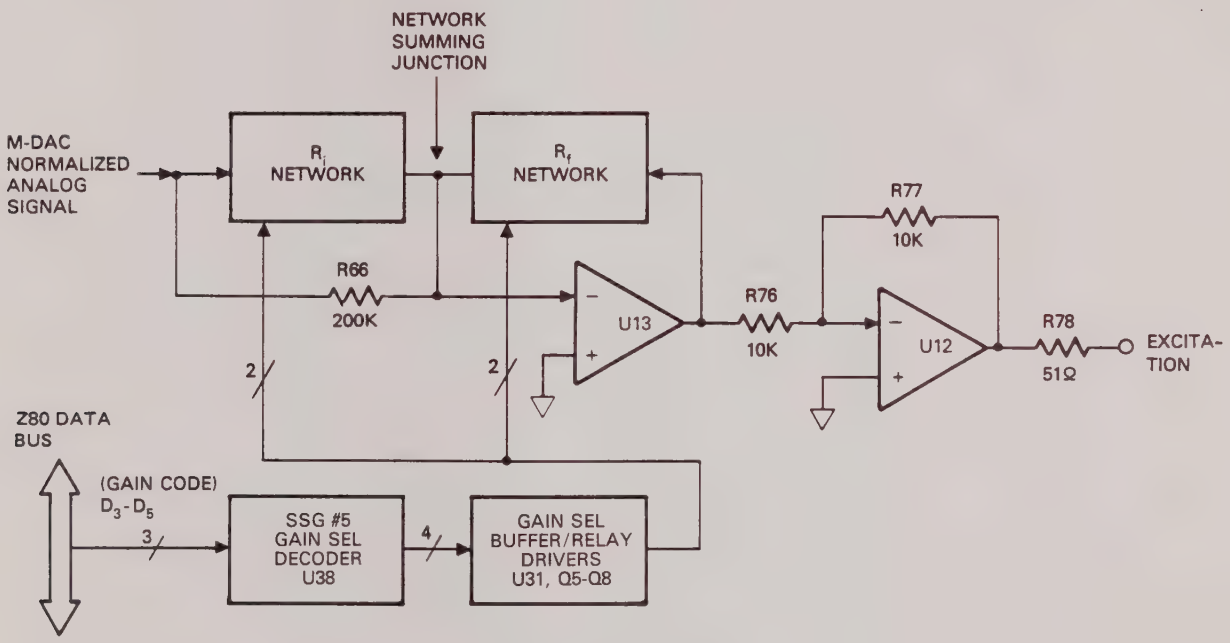

Figure 5-14. Gain Controlled Output Amplifiers Functional Block Diagram

SERVICE MANUAL

TV-50/90/120

Data Display Monitor

5-017-1035

REV. A Nov., 1977

Ball Electronic Display Division

BALL ELECTRONIC DISPLAY DIVISION P.O. BOX 43376 • ST. PAUL, MINNESOTA 55164 • TELEPHONE: (612) 786-8900 • TWX: 910-563-3552

PART 1

OPERATING DATA

This section of the service manual provides data concerning the specification, installation and operation of the TV 50, 90, and 120 Data Display Monitor.

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Section 1

GENERAL INFORMATION

1.1 GENERAL DESCRIPTION

The TV 50, 90 and 120 series monitor is a raster scan display designed specifically for data terminals. They are designed for high quality display of alphanumeric dot characters.

The data monitor accepts video, horizontal drive and vertical drive as separate TTL level signals, eliminating stripping circuits in the data display unit as well as mixing circuits in the external logic interface.

The 100% solid state silicon circuitry of the PWA provides cool operation and high reliability. The electronic package has been miniaturized for compatibility with small volume requirements.

1.2 ELECTRICAL SPECIFICATIONS

1.2.1 Input Data Specification

PWB Edge Input Connector: Viking - 2VK10S/1-2
Amphenol - 225-21031-101
Cinch - 250-10-30-170
BBRC No. - 1-039-0119

Video Input Amplitude : Low 0.0 + 0.4 - 0.0 volts
High 4.0 ± 1.5 volts

Video Pulse Width : 50ns or greater

Vertical Drive Rate : 49 to 61 Hz

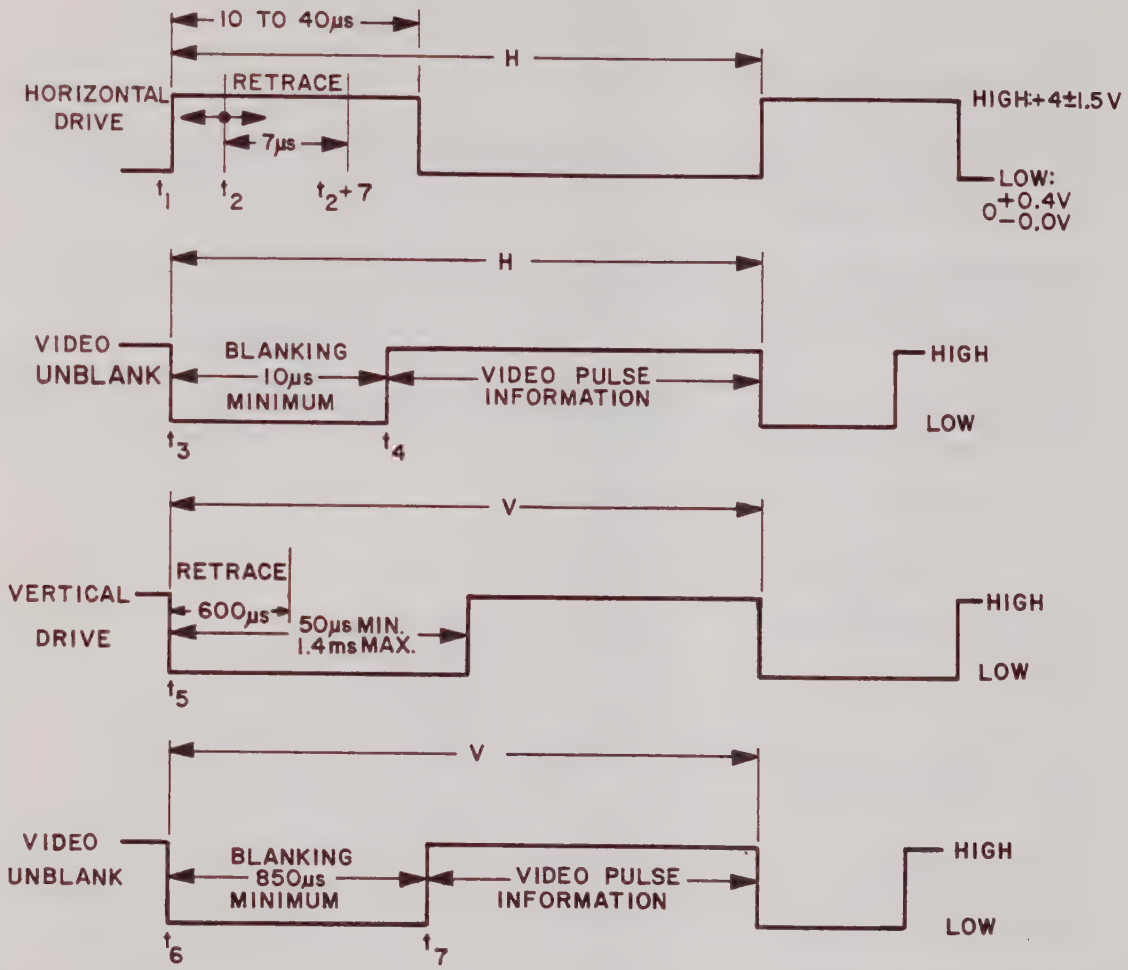
Horizontal Drive Rate : 15,250 to 16,250 Hz

Rise and Fall Times : Video Less than 20ns
Vertical Less than 100ns
Horizontal - Less than 50ns

Input Signal Format : Refer to figure 1-1

1.2.2 Data Display Specifications

Input Impedance:	Min Shunt Resistance	Max Shunt Capacitance
Video Input (Class A)	4k	40-60pF
Vertical Drive Input	1.2k	40pF
Horizontal Drive Input	510Ω	40pF



NOTES:

1. HORIZONTAL RETRACE IS INITIATED AT t_2 (1.5 TO 7.0μs AFTER t_1, DEPENDING ON SETTING OF A103).
2. VERTICAL RETRACE IS INITIATED AT t_5 WITHOUT DELAY.
3. H= PERIOD OF ONE LINE: 63.5μs ±3%.
4. V= PERIOD OF ONE FIELD: 16.4ms MIN. TO 20.4ms MAX.
5. VIDEO PULSE WIDTH SHOULD BE 50ns MIN.

TABLE 1. t_3 VS t_1 TIMING FOR CENTERED HORIZONTAL VIDEO AS FUNCTION OF H. BLANKING WIDTH.

HORIZONTAL VIDEO BLANKING	
WIDTH	LEAD / LAG
$t_4 - t_3$	$t_1 - t_3$
10μs	−5.5 TO 0μs
12μs	−4.5 TO 1μs
14μs	−3.5 TO 2μs
16μs	−2.5 TO 3μs
18μs	−1.5 TO 4μs
20μs	−0.5 TO 5μs

TABLE 2. t_6 VS t_5 TIMING FOR CENTERED VERTICAL VIDEO AS FUNCTION OF V. BLANKING WIDTH.

VERTICAL VIDEO BLANKING	
WIDTH	LEAD / LAG
$t_7 - t_6$	$t_5 - t_6$
850μs	125μs
900μs	150μs
1000μs	200μs
1200μs	300μs
1400μs	400μs

Figure 1-1 Synchronization and Blanking Generator Waveform

Video Amplifier:

Bandwidth	12 MHz - 3db (Class A mode)
Rise and Fall Time (10 to 90% amplitude)	Less than 35ns (linear mode)
Storage Time	15ns max (linear mode)

Retrace Time:

Vertical	600µs
Horizontal	7µs

1.2.3 Display Specifications

CRT Display (without bonded panel) Horizontal Resolution @ 15,750 Hz

Nominal Diagonal Measurement Inches/mm	Phosphor	*Resolution (TV lines)	
		Center	Corner
5/127	P4	650 @ 60 fL**	550 @ 60 fL**
9/229	P4	800 @ 40 fL	650 @ 40 fL
12/305	P4	900 @ 40 fL	750 @ 40 fL
12/305	P39	900 @ 20 fL	750 @ 20 fL

*Resolution is measured in accordance with EIA RS-375A except burst modulation is adjusted for 100% and burst frequency is then increased to the point where resolution of the lines is just discernible.

**Set reference black to visual cutoff with brightness control and reference white to the indicated fL with contrast control.

1.2.4 Geometric Distortion Specifications

On-Axis Scan Non-Linearities - No picture elements displaced from true position by more than 2% of active raster height. Measurement made using "EIA Linearity Chart" in accordance with RS-375A.

If measured on a field of characters, the character height and width are within 10% of that for any adjacent character and within 20% of that for any character on screen

Perimeter Non-Rectangularity - The perimeter of a full field of characters approaches an ideal rectangle of 4 by 3 aspect ratio to within ±1.5% of the rectangle height.

1.2.5 Power Requirements

AC Models	120V	220V/240V
Voltage:	105-130 VRMS ±10%	220 or 240 VRMS ±10%
Frequency:	49-61Hz	49-61Hz
Power:	24 Watts Nominal	24 Watts Nominal
Fuse:	2A	2A

DC Models	12VDC	15VDC
Voltage:	12±0.2 VDC	15± 0.2 VDC
Ripple:	100 mV p-p for refresh synchronous with power freq.	
	10 mV p-p for refresh non-synchronous with power freq.	
Current:	750 mA DC nominal	900mA DC nominal
	1.0 A DC maximum	1.5 A DC maximum
Fuse:	2A	2A

MATING CONNECTORS REQUIREMENTS

Power (AC models only): 4-contact male connector shell (Molex 03-06-1041) with female contact (Molex 4529T).

Signal (and power for DC models): 10-contact board edge connector (Refer to paragraph 1.2.1 for details.)

WARNING
ANY POWER TRANSFORMER MUST BE WELL REMOVED FROM CRT AND/OR BE OF LOW EXTERNAL FLUX FIELD DESIGN

1.3 MECHANICAL SPECIFICATIONS

Table 1-1 and figure 1-2 lists the mechanical specifications for the TV 50/90/120 Data monitor. For further information, contact our General Sales Offices. They are:

Addison, Illinois (312) 279-7400
Ocean, New Jersey (201) 922-2800
Santa Clara, California (408) 244-1474
Upland, California (714) 985-7110

1.4 ENVIRONMENTAL SPECIFICATIONS

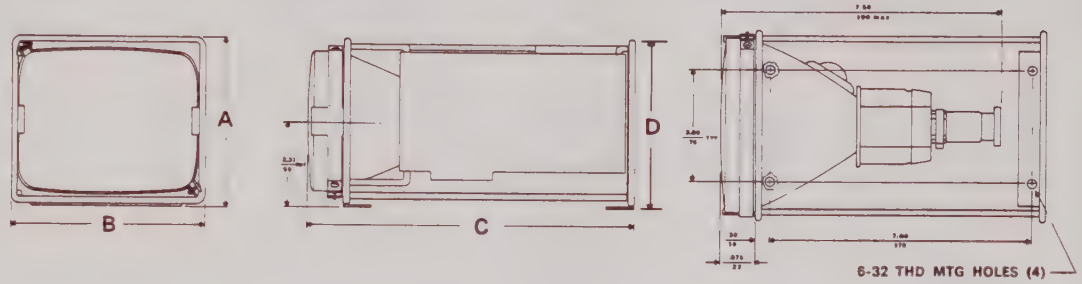
	OPERATING RANGE	STORAGE RANGE
Temperature (Ambient)	5°C to 55°C	-40°C to 65°C
Humidity (Non-Condensing)	5 to 80%	5 to 90%
Altitude	Up to 10,000 ft/ 3048m	Up to 30,000 ft/ 9144m

MODEL		TILT	* DIMENSIONS (Inches/Millimeters) A	B	C	D	WEIGHT Lbs/kg	OUTLINE NO
TV50	DC	0°	4.56/116	5.12/130	8.62/219	4.56/116	3.0/1.4	2-030-0319
TV90	DC	0°	7.00/178	9.50/241	9.75/248	6.16/156	6.8/3.1	2-030-0401
TV90	AC	0°	7.00/178	9.50/241	9.75/248	6.16/156	10.1/4.6	2-030-0401
TV90	DC	10°	6.90.175	9.50/241	9.75/248	6.16/156	6.8/3.1	2-030-0401
TV90	AC	10°	6.90/175	9.50/241	9.75/248	6.16/156	10.1/4.6	2-030-0401
TV120	DC	0°	9.06/230	11.40/289	11.84/301	5.75/146	11.0/5.0	2-030-0400
TV120	AC	0°	9.06/230	11.40/289	11.84/301	5.75/146	13.4/6.1	2-030-0400
TV120	DC	5°	9.03/229	11.40/289	11.84/301	5.75/146	11.0/5.0	2-030-0398
TV120	AC	5°	9.03/229	11.40/289	11.84/301	5.75/146	13.4/6.1	2-030-0398
TV120	DC	7½°	9.00/229	11.40/289	11.84/301	5.75/146	11.01/5.0	2-030-0399
TV120	AC	7½°	9.00/229	11.40/289	11.84/301	5.75/146	13.4/6.1	2-030-0399
TV120	DC	10°	8.92/227	11.40/289	11.84/301	5.75/146	11.01.5.0	2-030-0397
TV120	AC	10°	8.92/227	11.40/289	11.84/301	5.75/146	13.4/6.1	2-030-0397
TV120	DC	15°	10.25/260	11.40/289	11.88/302	10.25/260	10.5/4.8	2-030-0396
TV120	AC	15°	10.25/260	11.40/289	11.88/302	10.25/260	12.9/5.9	2-030-0396

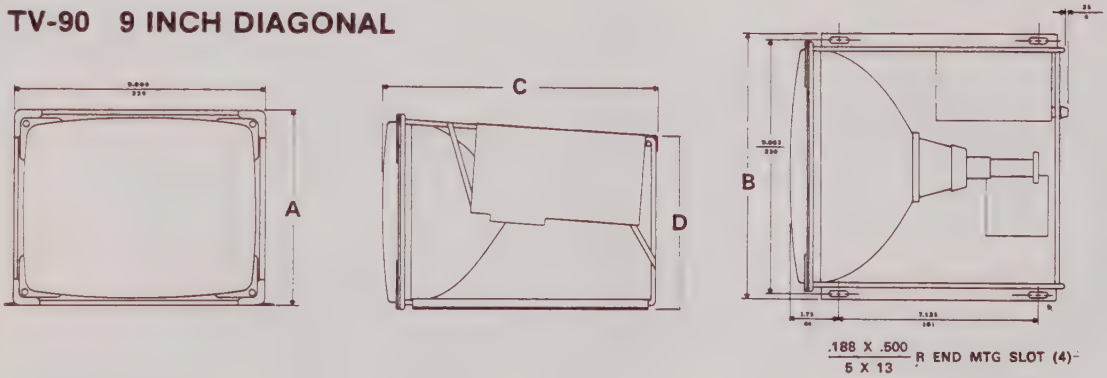
Table 1-1 Mechanical Specifications

DIMENSIONS

TV-50 5 INCH DIAGONAL



TV-90 9 INCH DIAGONAL



TV-120 12 INCH DIAGONAL

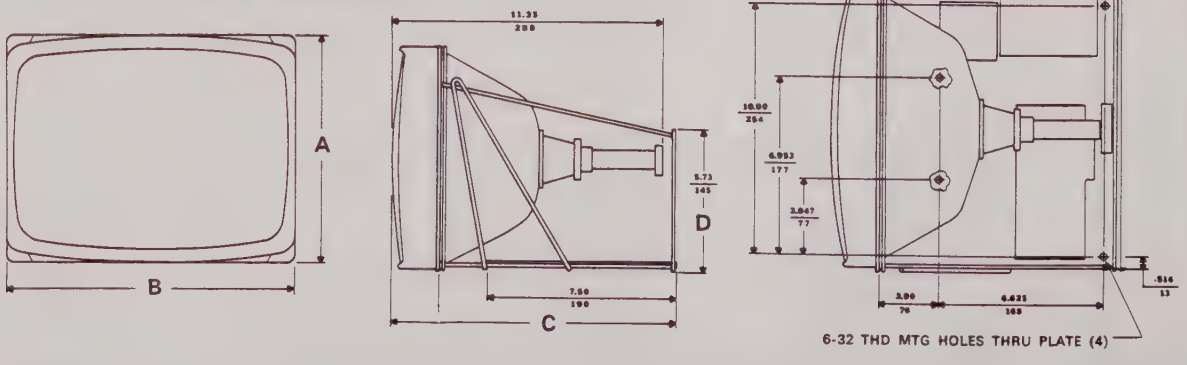


Figure 1-2 TV50, 90, 120 0° tilt with bonded panel dimensions

1.5 HUMAN FACTORS SPECIFICATION

X-Ray Radiation

The TV 50, 90 and 120 Data monitor complies with the Federal Regulation for Radiation Control as required by the Radiation Control for Health and Safety Act of 1968, and as implemented by Title 21, Subchapter J of the Code of Federal Regulation.

These regulations place certain requirements upon manufacturers of products which can emit x-rays under some conditions of operation or failure. This includes CRT data display monitors.

Label Visibility

Certification of compliance with radiation regulations is shown by a label attached to each monitor. The user is responsible for labeling his product in a similar fashion or in making the DHEW label easily visible from the outside of the enclosure. The regulations state that "This (certification) information shall be provided in the form of a tag or label permanently affixed or inscribed on such product so as to be legible and readily accessible to view when the product is fully assembled for use..." Each monitor is supplied with an extra label attached to the face of the CRT. The user will remove this label and use it as stated above.

Power Requirements

The Data monitor is designed to operate and meet radiation requirements when operated within the respective AC or DC input power specifications. Radiation testing is performed at the maximum specified input voltage for AC powered monitors or at 130 VAC for those nominally powered at 110-120 VAC, 60 Hz.

DC powered monitors have an additional requirement because the DC source is usually regulated and subject to failure of the series pass element. This can result in an appreciable increase in the anode voltage and consequent emission of x-rays. This is not a problem for monitors equipped with over voltage protection. For monitors not so equipped, it is necessary for the buyer to ensure that the normal adjustment of his regulator does not exceed the maximum level specified for the particular monitor. Furthermore, he shall ensure that the maximum available voltage from the supply cannot exceed 1.33 times nominal monitor input when the supply has a single failure such as to cause the highest possible output voltage.

User Operating Controls

The only external control required for operation of the TV 50, 90, and 120 display unit is the contrast control. This control is a carbon composition variable resistor, 500Ω±20%; ¼ watt.

The brightness control is mounted on the printed wiring board and is an internal adjustment by the user. An option is available where this control is removed from the board and a remote brightness control supplied by the user is utilized. The remote brightness control is a carbon composition variable resistor, 100kΩ±20%; ¼ watt.

Section 2

INSTALLATION

2.1 MECHANICAL

The TV 50 data monitor has four 6-32 clinch nuts for mounting the unit. The TV 120, 0°, 5°, 7½° and 10° monitors have four 6-32 clinch nuts on the frame for installation purposes. The TV 120, 15° monitor uses three 6-32 clinch nuts for mounting. The TV 90 data monitor has four .188X.500 radius end slots for installation. Refer to figure 1-2

2.2 ELECTRICAL

2.2.1 DC Input

The TV 50/90/120 DC models can be operated from either a 12 VDC or 15 VDC source. Refer to section 1.2.5 for details. The DC input power is applied through the 10 pin edge connector.

2.2.2 AC Input

The TV 90/120 AC models have their own self contained AC power supply. This supply can operate either on 120 VAC or 220/240 VAC depending on which plug of the jumper plug assembly P2 is inserted into the power supply module.

The power transformer is wired to operate on either 120 VAC or 220/240 VAC 50/60Hz. To operate the power supply on 120 VAC, take the connector shell of P2 marked with 120 and insert it in to J2. Conversely, to operate at 220/240 VAC insert the connector shell of P2 marked with 240 into J2.

AC power is supplied to the unit via J1. J1 is a 4 contact female connector shell (Molex #03-06-2041) with male contacts (Molex #45295)

2.3 Location

The TV 50/90/120 models shall not be located in an area that restricts air flow around the unit nor shall it be placed near any heat generating sources, since this may cause the unit to overheat.

2.4 GROUNDING TECHINIQUES

The method of interconnecting and grounding the equipment is a function of the signal frequency. Optimum grounding depends largely on the system in which the equipment is used. The following grounding technique is recommended when installing the monitor. Refer to figure 2-1 for interface connections.

The horizontal, CRT arc and video/vertical board circuit grounds are terminated at J101. The horizontal ground (J101-1) and CRT arc ground (J101-5) is connected together by a jumper wire on the board and they are connected to the frame by a wire from E110.

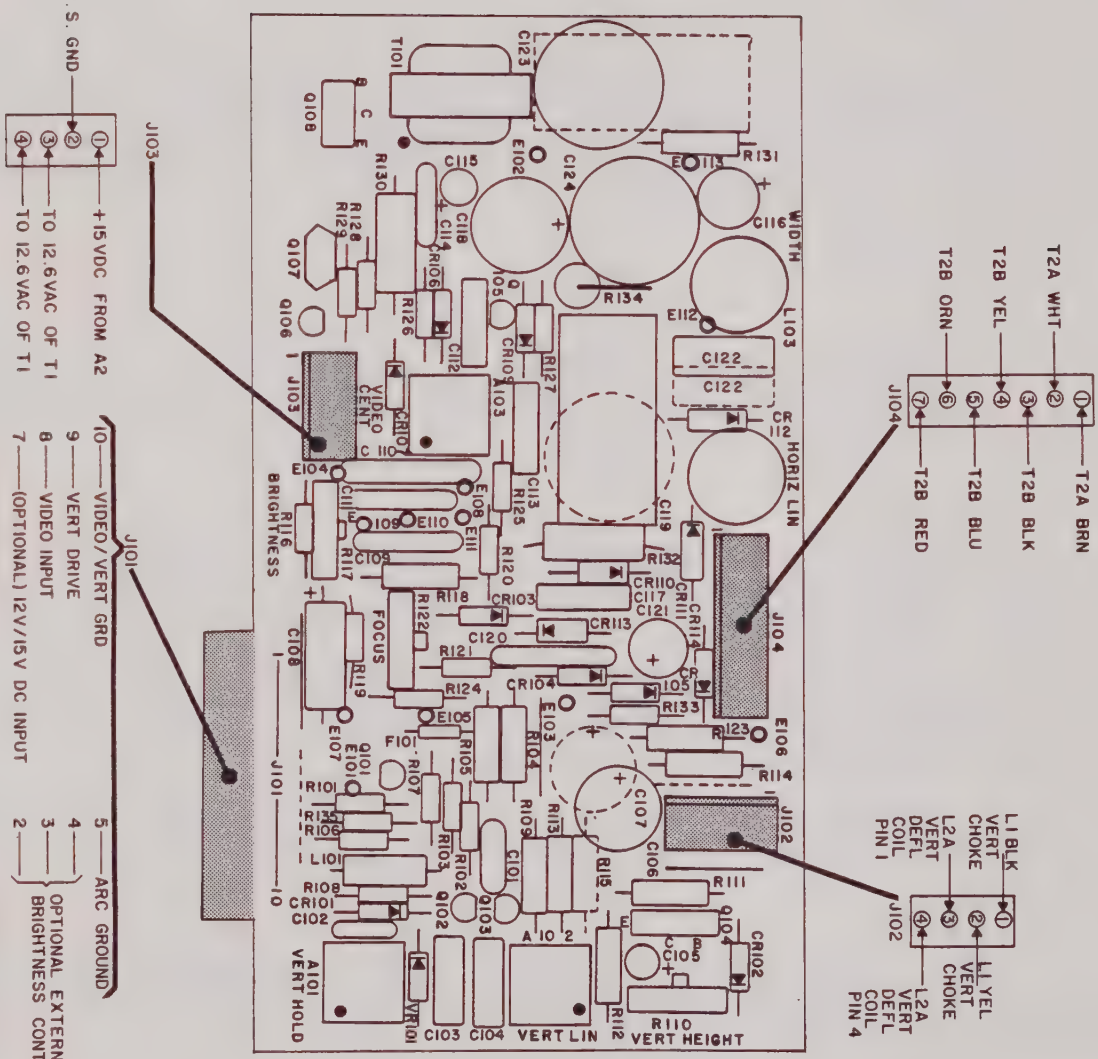


Figure 2-1 Interface Connections

A connection to system ground must be made at both J101-1 and J101-10. When the frame is an integral part of system ground, one of three possible ground configurations can be used.

1. When a good electrical ground connection cannot be made between the monitor frame and system ground, then J101-1 and J101-10 is wired separately to the system ground.

2. When a good ground connection can be made between the monitor frame and system ground, then J101-10 is wired to the system ground and J101-1 is left open.

3. When the ground connection between the monitor frame and the system ground is acceptable and it is desired to omit the wire from J101-10, then add a jumper wire to the board to connect J101-5 and J101-10 together. J101-5 is then wired to the system ground. The monitor is normally supplied without the jumper wire from J101-5 to J101-10 to prevent horizontal circuit ground currents from flowing in the video ground circuit.

In cases of severe arc related problems, the jumper between J101-1 and J101-5 can be removed and J101-5 or E110 can be connected separately to the frame or CRT aquadag ground. J101-1 or E102 must then be connected either to the frame or system ground.

To isolate the frame from system ground, J101-1 and J101-10 should be wired separately to system ground. Add another wire to J101-1 and connect it and J101-5 to the frame (aquadag ground) through a capacitor. The frame cannot be completely isolated, since an AC connection between the signal ground and frame must be maintained to assume a complete circuit for the CRT aquadag capacity.

When the video is routed in by a long cabling, shielded cable should be used. To avoid a ground loop, only one end of the shield should be grounded.

2.5 INPUT SIGNAL LEAD ROUTING

The input signal leads probably will carry high frequency signals and should be given the following considerations:

A. To minimize distributed capacity and capacitive pickup of nearby radiated fields, route the video leads separately and away from all other wiring.

B. Make the lead length as short as possible, consistent with the packaging requirements.

C. Ideally, the video line should meet the requirements of a terminated coaxial system; i.e., the video line should exhibit a constant impedance from source load.

Section 3

OPERATION

3.1 GENERAL

After power, video and drive signals have been applied to the monitor, the contrast and brightness controls may be adjusted to provide the optimum display.

3.2 BRIGHTNESS ADJUST

The monitor is used to display alphanumeric information. The video polarity is usually white characters on a black background. The brightness control should then be adjusted for visual cutoff of the raster. A maximum contrast ratio can now be obtained when video is applied.

3.3 CONTRAST ADJUST

The video amplifier is designed to operate linearly from +.65 to +2.5 V signal input. The contrast control should be adjusted to the point where defocusing sets in and then backed down slightly. This occurs at a 15-20V p-p video swing at the CRT cathode for the TV90/120, and at a 12-15V p-p swing for the TV50. In no case should contrast be adjusted to cause saturation of Q101, as this impairs the pulse response of the video amplifier.

PART II

SERVICE DATA

Section 4 through 6 and the supplement are for qualified service personnel.

The TV 50, 90, 120 has no end user serviceable parts inside. Refer service to qualified service personnel.

Section 4

THEORY OF OPERATION

4.1 VIDEO AMPLIFIER

The video amplifier consists of Q101 and its associated circuitry. The incoming video signal is applied to the monitor through J101-8 and R101 to the base of Q101.

Transistor Q101 has a nominal gain of 15, and operates as a class B amplifier. Q101 remains cutoff until a DC coupled, positive-going signal arrives at its base and turns it on. R103 provides series feedback which makes the terminal to terminal voltage gain relatively independent of transistor parameters and temperature variations. R102 and C101 provide emitter peaking to extend the bandwidth to 12MHz.

The negative going signal at the collector of Q101 is direct coupled to the CRT cathode. The class B biasing of Q101 allows a large video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is also determined by the negative potential at its grid which is varied by the brightness control.

4.2 VERTICAL DEFLECTION

Q102 is a thyristor used as programmable unijunction and together with its external circuitry forms a relaxation oscillator operating at a vertical rate. The sawtooth forming network consists of A101, C103 and C104. These capacitors charge exponentially until the voltage at the anode of Q102 exceeds its gate voltage at which time Q102 becomes essentially a closed switch, allowing a rapid discharge through L101. The rate of charge or frequency is adjustable by A101. The oscillator is synchronized by a negative pulse coupled to its gate from the vertical drive pulse applied externally at J101-9.

A divider network internal to A101 sets the free running frequency by establishing a reference voltage at the gate. This programs the firing of Q102 and amounts to resistive selection of the intrinsic standoff ratio. The frequency is controlled by passive components only. CR101 provides temperature compensation for Q102 while controlling the gate impedance to allow easy turn on and off of Q102. L101 forms a tuned circuit with C103 and C104 during conduction of Q102 which provides a stable control on the drop-out time of Q102 to assist in maintaining interlace. Q103 collector to base forward diode clamping action prevents the voltage from swinging too far negative during this flywheel action.

The sawtooth at the anode of Q102 is direct coupled to the base of Q103. This stage functions as a darlington pair emitter follower driver for the output stage Q104. It presents an extremely high impedance in shunt with A101 and prevents the Beta dependent input impedance of Q104 from affecting the frequency of the

sawtooth forming network.

Linearity control of the sawtooth is accomplished by coupling the output at Q103 emitter resistively back into the junction of C103 and C104. This provides integration of the sawtooth and inserts a parabolic component. The slope change rate of the sawtooth at Q103 output is controlled by the setting of A102. The output at Q103 is coupled into a resistive divider..

Height control R110 varies the amplitude of the sawtooth voltage applied to the base of Q104 and controls the vertical raster size on the CRT. C105 is used to limit the amplitude of the flyback pulse at Q104 collector.

The vertical output stage Q104 uses an NPN power transistor operating as a class AB amplifier. The output is capacitively coupled to the yoke. L1 provides a DC connection to B+ for Q104; it has a high impedance compared to the yoke inductance which causes most of the sawtooth current of Q104 to appear in the yoke. R114 prevents oscillations by providing damping across the vertical yoke coils.

4.3 HORIZONTAL DEFLECTION

4.3.1 Low Level Stages (Figure 4-1)

The purpose of Q105 and Q106 is basically to process the incoming horizontal drive signal into a form suitable to drive the output stage Q108. The duty cycl of Q108 becomes essentially independent of the amplitude and pulse width of the drive pulse. This is a necessary condition to assure stability and reliability in the output stage. In adddition, these stages provide a horizontal video centering adjustment by delaying retrace with respect to the horizontal drive pulse.

The drive pulse is presented to Q105 via J101-6. The base circuit of Q105 includes a clamp and a differentiator which makes Q105 output insensitive to drive pulse amplitude and width changes. The only requirement is that pulse amplitude be of 2.5 volts minimum and pulse width should be 10-40µs. Q105 together with Q106 functions as a monostable multivibrator with Q107 being a slave that provides a positive feedback. Specifically, when Q105 is turned on by the drive pulse, it discharges C112 at a rate determined by the setting of A103. When C112 is discharged to 2.75 volts, Q106 turns off. This change of state turns Q107 on and the base drive to Q106 from R128 is shunted thru Q107. Q106/Q107 remains in this state for nominally 25µs until C112 recharges through A103 to 8.25 volts. At this time, Q106 is biased on again by the current through A103. The multivibrator is now in a state that Q106 is on and Q105/Q107 is off. It will remain in this state until the next drive pulse occurs or power is turned off. C112 is the only timing capacitor in the circuit and has two time constants associated with it. Primarily, the charge path between pin 1 and pin 3 of A103 determines the on time of Q107 while the discharge path through the video centering control and Q105 determines the delay between application of the drive pulse and start of retrace (turn on of Q107).

4.3.2 High Level Stages

These stages consist of Q107 driving the output stage, Q108 and its associated

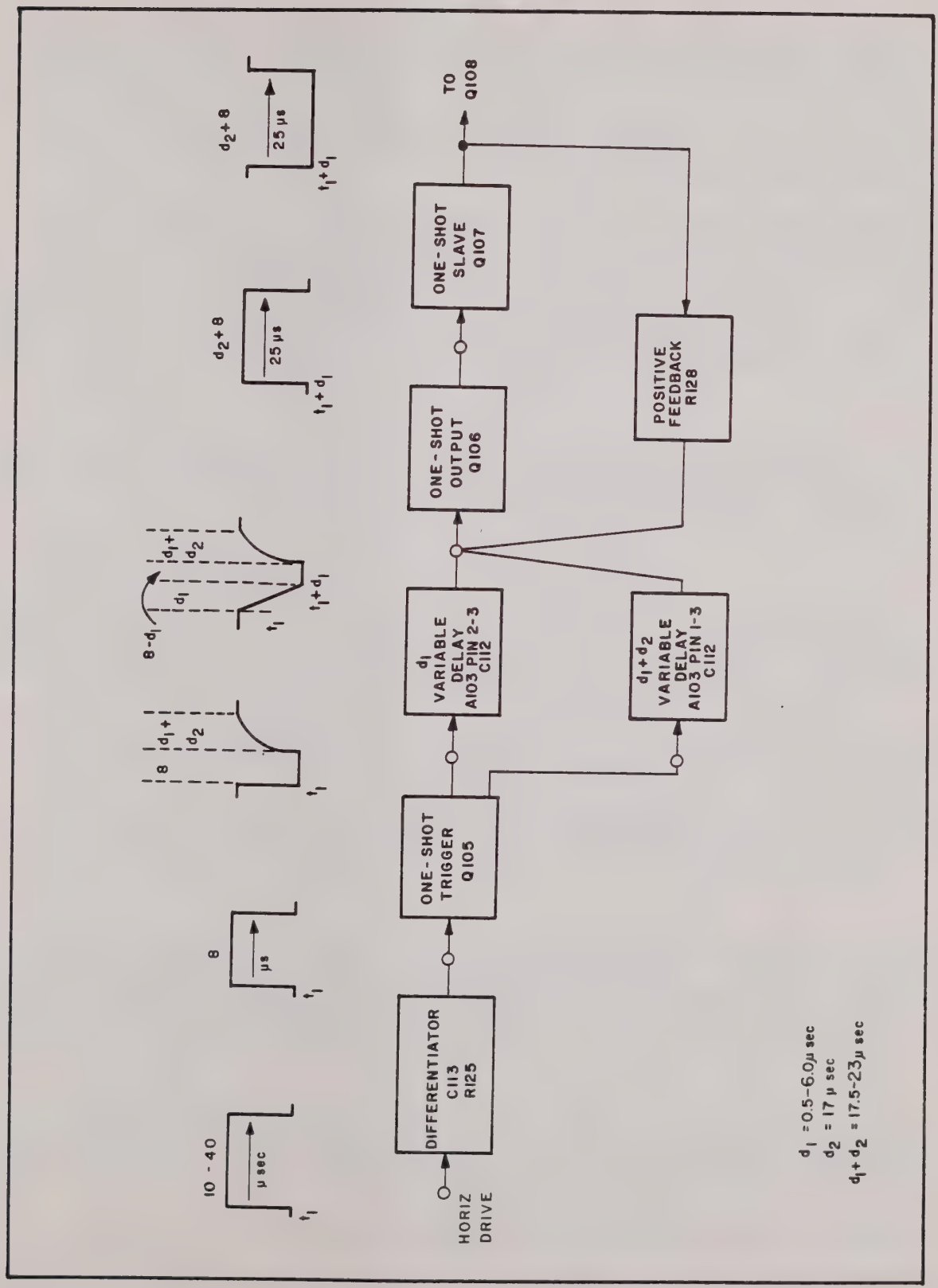


Figure 4-1 Horizontal Drive Processing and Timing Chart

circuitry thru T101. Q107 is an inverting slave of Q106 and is driven alternately into saturation and cutoff as are all stages in the horizontal circuit. Q107 output is transformer coupled to the output stage with phasing of T101 chosen such that Q108 turns off when Q107 turns on. This allows Q108 to turn off quickly, thus minimizing dissipation. A careful review will show that Q108 turns off at a variable delay time after receipt of the drive pulse. This action causes retrace to begin.

During conduction of the driver transistor, energy is stored in the coupling transformer. The polarity at the secondary is then phased to keep Q108 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q107 into cut off, the secondary voltage changes polarity. Q108 now saturates due to the forward base current flow. This gradually decreases at a rate determined by the transformer inductance and circuit resistance. However the base current is sufficient to keep Q108 in saturation until the next polarity change of T101.

The horizontal output stage has two main functions: 1) to supply the deflection coil with the correct horizontal scanning currents: 2) to develop high voltage for the CRT anode and DC voltage for the CRT bias, focus and accelerating grids as well as the DC voltage for the video output stage.

Q108 acts as a switch which is turned on or off by the rectangular waveform on the base. When it is turned on, the supply voltage plus the charge on C123 causes deflection current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a polarity change of T101 which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle negative voltage pulse is developed by the deflection coil inductance and the primary of T2. The peak magnetic energy which was stored in the deflection coil during scan time is not transferred to C122 and the deflection coil distributed capacity. During this cycle, the beam is returned to the center of the screen.

The charged capacitances now discharge into the deflection coil and induce a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the coil moves the scanning beam to the left of the screen.

After slightly less than half a cycle, the decreasing voltage across C122 biases the damper diode CR111 into conduction and prevents the flyback pulse from further oscillation. The magnetic energy that was stored in the deflection coil from the discharge of the distributed capacity is now released to provide sweep for the left half of scan and to charge C123 through the rectifying action of the damper diode. The beam is now at the center of the screen. The cycle will repeat as soon as the base of Q108 becomes positive with respect to its emitter.

C123 serves to block DC current from the deflection coil and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not follow the same arc.

L103 is an adjustable width control placed in a series with the horizontal de-

flection coils. The variable inductance allows a greater or lesser amount of deflection current to flow through the horizontal yoke and varies the width of the horizontal scan.

Linearity control is provided by modifying the deflection coil voltage. During retrace, an auxilliary winding on the flyback transformer supplies a pulse which charges C119 through rectifier diode CR112 and L102. This voltage is then applied in series with the deflection coil when the damper diode turns on at the start of trace. The voltage is sawtooth shaped and has the effect of decreasing the deflection coil current as a function of the sawtooth shape. This compensates for the stretch normally found on the left side of the screen due to the deflection coil and system RL time constant. Linearity is optimized by adjustment of L102 which acts as an impedance to the pulse from T2.

The negative flyback pulse developed during horizontal retrace time is rectified by CR110 and filtered by C117. This produces approximately -130 VDC which is coupled through the brightness control R117 to G1 of the CRT.

This same pulse is transformer-coupled to the secondary of T2 where it is rectified by CR2, CR113 and CR114 to produce rectified voltage of approximately 12KV, 400V and 32V respectively. 12KV is the anode voltage for the CRT, while 32V is used for the video output stage, and the 400V source is used for G2 and G4 voltages for the CRT.

4.4 LOW VOLTAGE SUPPLY

The TV 90/120 models are available with an internal power supply. This supply utilizes an integrated circuit voltage regulator which supplies 15VDC±2.5% to J103-1. It also supplies 12.6 VAC to J103-3 and 4 for the CRT filament.

The 120VAC primary voltage (220/240V optional) is stepped down at the secondary of T1 where it is rectified by CR1 and filtered by C1. A2 functions as a series regulator to drop the rectified voltage down to 15V at pin 2. The regulator maintains a constant output voltage (within 2.5%) with changes in line voltage load or temperature. It is capable of supplying 1.5 amps and features internal current limiting, thermal shutdown and safe over-voltage protection. A hermetically sealed TO-3 case is used for high reliability and low thermal resistance.

If a short circuit is present at the output, the current limiting feature of A2 will cause the output current to fold back to safe levels. The fast limiting action of A2 is very effective in protecting transistors from abnormal loads. The resistor R1, is used to reduce the power dissipation in A2.

Section 5

ADJUSTMENT AND MAINTENANCE

5.1 HORIZONTAL ADJUSTMENTS

With a crosshatch signal applied, adjust video centering control, A103 to center the video within the raster horizontally. Adjust L102 for best horizontal linearity. Do not adjust L102 core out farther than necessary as this causes excessive power to be consumed.

Adjust L103 for desired width.

5.2 VERTICAL ADJUSTMENTS

With the crosshatch signal applied, adjust vertical hold control A101 to lock in the picture.

Adjust vertical linearity control A102 for best overall linearity. This control affects the vertical frequency slightly and might require a readjustment of the hold control. Adjust vertical height control R110 for desired height.

5.3 FOCUS ADJUST

Adjust focus control R122 for best overall focus of the picture. Usually the center and corners of the screen do not focus at the same setting and a compromise must be made.

5.4 CENTERING ADJUST

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke. The ring magnets should not be used to offset the raster from its nominal center position because this degrades the focus and resolution of the display and may cause neck shadow.

If the picture is tilted, rotate the entire yoke.

5.5 TROUBLESHOOTING GUIDE

Symptom	Possible Remedy
1. Screen is dark	Check 15V bus, Q108, Q107, CR2, CR113
2. Loss of Video	CR114, Q101
3. Power consumption is too high	Check horizontal drive waveform; adjust horizontal linearity coil; Q107, Q108

4.	Low voltage bus incorrect (for units with a low voltage supply)	A1, A2 NOTE: Low voltage supply will indicate low or "0" volts if an abnormal load is evident on the 15 volt line.

5.6 RASTER SHIFTING

The extra cost factory option of inserting R113 or R115 makes possible a fixed raster shift either down or up by allowing a fixed DC current to flow in the deflection coil. This option precludes the need for using the centering rings for non-standard centering which would result in disturbance of geometry and focus.

1. Raster pull down (Refer to figure 5-1)

   Add R113 from J102-4 to ground in holes provided. Value to be selected for desired amount of pull down.

2. Raster pull up (Refer to figure 5-1)

   Replace C106 with a jumper wire. Remove jumper wire from J102-3 and J102-1 and replace with C107, 470uf, 10v, electrolytic. Add R115 from J102-3 to ground in holes provided. Value of R115 to be selected for desired amount of pull up.

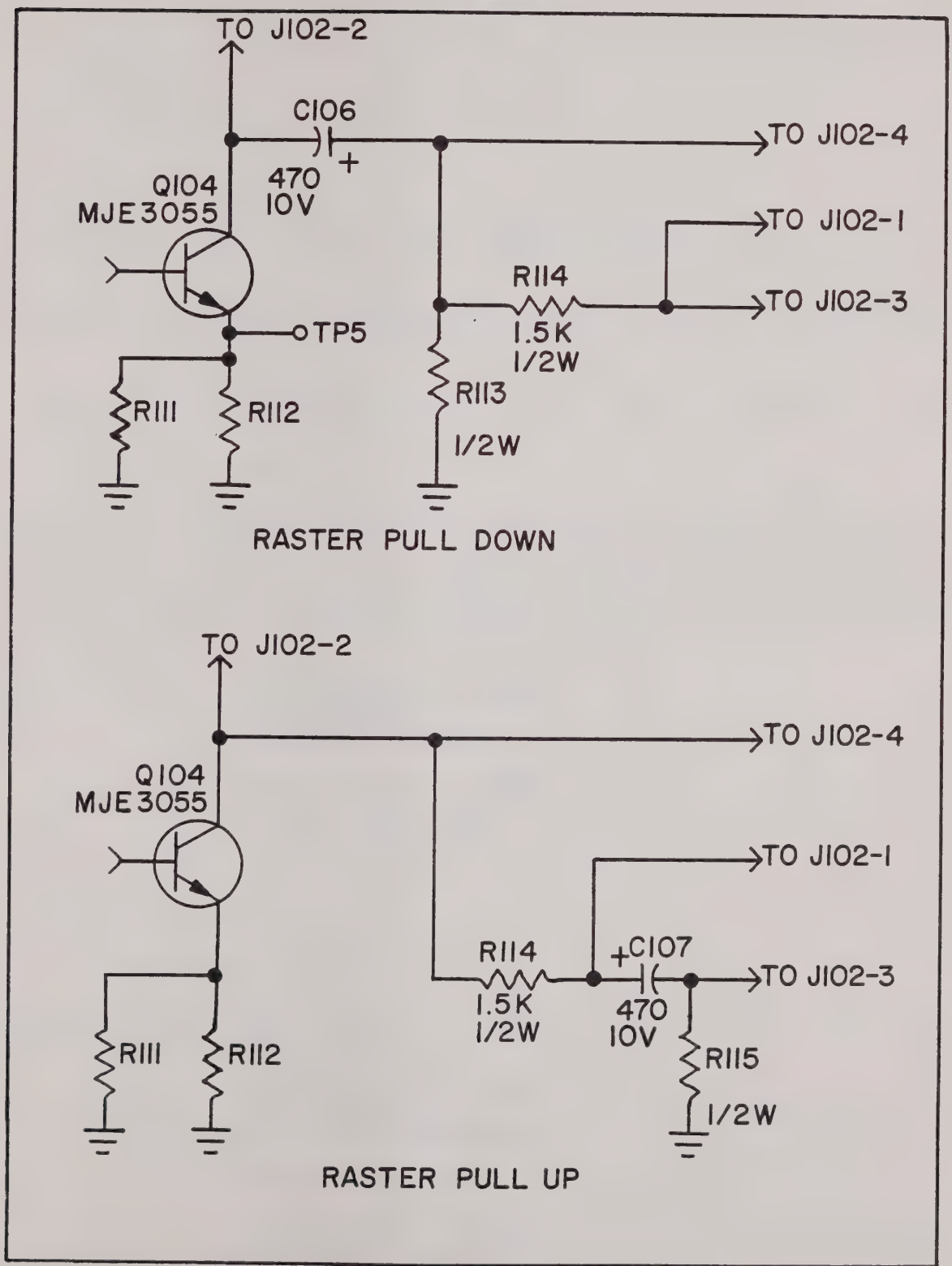


Figure 5-1 Schematic for Raster Shifting

Section 6

SERVICE DATA

6.1 GENERAL

This section contains the replaceable electrical parts list, schematic, PWB component layout and waveforms for servicing of the TV 50, 90, 120 data monitor.

If a part you have ordered has been replaced with a new part or an improved part, our customer service representative will contact you concerning any change in the part.

Change information concerning the TV 50, 90, 120 units is located at the rear of the manual in the supplement section.

6.2 ORDERING PARTS

Most parts contained in the monitor are available commercially from electronic parts outlets. When it is necessary to order spare or replacement parts from BBRC, Electronic Display Division (E.D. DIV.), include the part description, part number, model and serial number data of the monitor as listed on the serial number plate and, if applicable, the schematic reference number listed in the parts list. Orders for these parts should be sent to:

Ball Electronic Display Division
P.O. Box 43376
St. Paul, Minnesota 55164

For rapid service:
Telephone area (612) 786-8900
or
TWX area (910) 563-3552

6.3 RETURNING PARTS

When the monitor requires service or repair in accordance with the enclosed warranty, return the unit or part to:

Ball Electronic Display Division
4501 Ball Road N.E.
Circle Pines, Minnesota 55014

ATTN: Customer Service

Telephone area (612) 786-8900
TWX area (910) 563-3552

Unnecessary delays may be avoided when parts are returned to Electronic Display Division using the following procedures:

(1) Package the unit or part in accordance with the method of shipment. Enclose a list of the material being returned and the reason for returning it.

(2) Send the unit or part, transportation prepaid, to the address stipulated for returning parts.

All equipment and parts described in the warranty will be replaced, provided E.D. DIV's examination discloses that the defects are within the limits of the warranty. If damages or defects are not within the limits of the warranty, the customer will be notified of the extent of repairs required and the cost. The unit will be repaired and returned upon agreement.

6.4 WAVEFORMS

The waveforms on the component layout were taken with 1.5 V peak to peak cross-hatch signal applied to the monitor. These waveforms can be used as a check point to localize problems to a specific circuit area. The waveform photographs indicate the actual peak amplitude for each test point. The TV 50 is the only exception, the peak to peak amplitude is specified for TP9, TP12, TP13 and TP14.

6.5 BOARD ASSEMBLY

The board assembly part number has a 6-002-XXXX prefix. The last four digits of the part number is found under the "use on 6-002" column in the parts list. The last four digits of the board assembly part number is stamped on the component side of the board near J101.

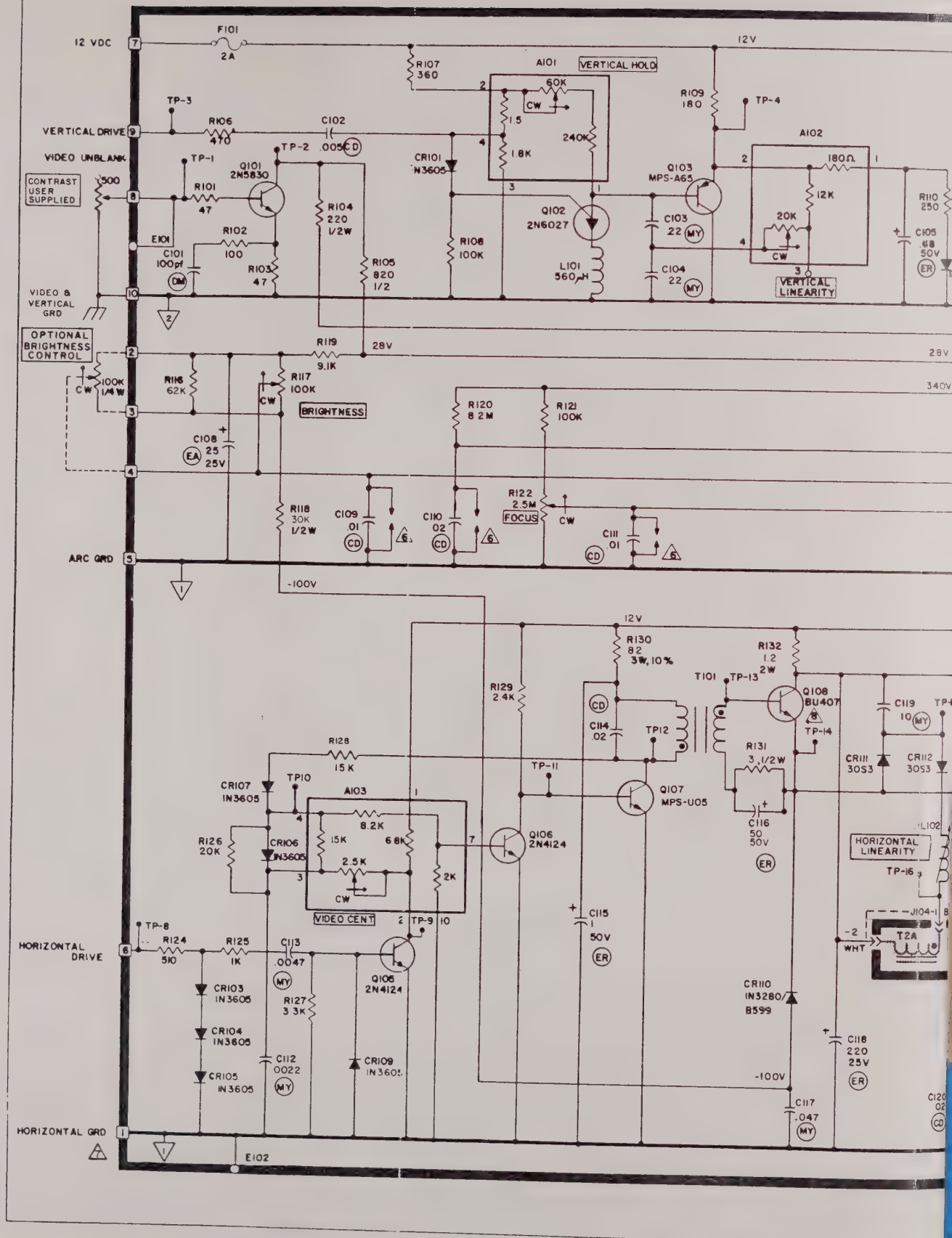
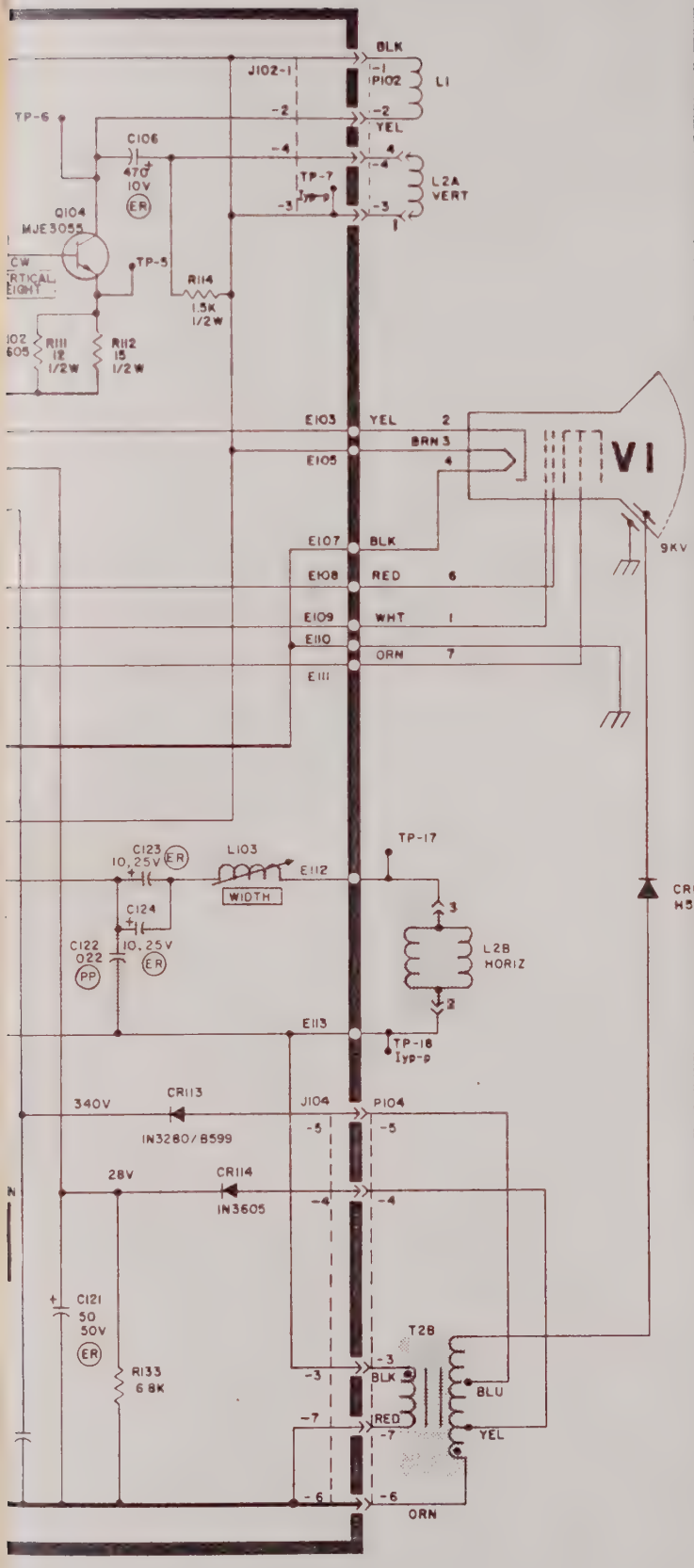


Figure 6-1 TV50



GENERAL NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS 1/4W, 5%, VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS. FOR CAPACITOR TYPES, SEE NOTE #9.
3. ☐ DENOTES J101 PC CARD EDGE CONNECTOR.
4. →→ DENOTES CONNECTION TO OFF BOARD COMPONENTS
5. REFERENCE DESIGNATION NOT USED: R113, R115
   LAST REFERENCE DESIGNATION USED: R133, C124
6. PROTECTIVE ARC GAPS ARE AN INTEGRAL PART OF PRINTED WIRE BOARD.
7. THE PWB CIRCUIT GROUNDS ARE BROUGHT OUT SEPARATELY TO PINS 1, 5 AND 10 OF J101. PWB CIRCUIT GROUNDS FOR PINS 1 AND 5 OF J101 ARE CONNECTED TOGETHER BY A JUMPER WIRE ON THE BOARD AND ARE CONNECTED TO CHASSIS GROUND VIA A WIRE FROM E110.

   THE DATA DISPLAY UNIT IS CONNECTED TO THE SYSTEM GROUND THROUGH PINS 1 AND 10 OF J101. FOR NON-STANDARD GROUNDING TECHNIQUES REFER TO SECTION 2 OF THE SERVICE MANUAL
8. ⏚ DENOTES HEATSINK
9. (DM) = DIPPED MICA
   (CD) = CERAMIC DISC.
   (MY) = MYLAR
   (EA) = ELECTROLYTIC AXIAL
   (ER) = ELECTROLYTIC RADIAL
   (PP) = POLYPROPYLENE

PRODUCT SAFETY MUST BE CONSIDERED WHEN ANY COMPONENT IS REPLACED IN THIS MONITOR. THE CRITICAL COMPONENTS THAT AFFECT X-RADIATION ARE DENOTED IN THE SHADED AREAS ON THE SCHEMATIC. COMPONENTS IN THE SHADED AREA ARE TO BE REPLACED ONLY WITH EDD DIV. APPROVED COMPONENTS.

THE USE OF SUBSTITUTE COMPONENTS WHICH DO NOT HAVE THE SAME CHARACTERISTICS AS THE EDD DIV. ORIGINAL COMPONENTS MAY CREATE EXCESSIVE X-RADIATION.

Ball — ELECTRONIC DISPLAY DIVISION

TITLE: SCHEMATIC
TV-50

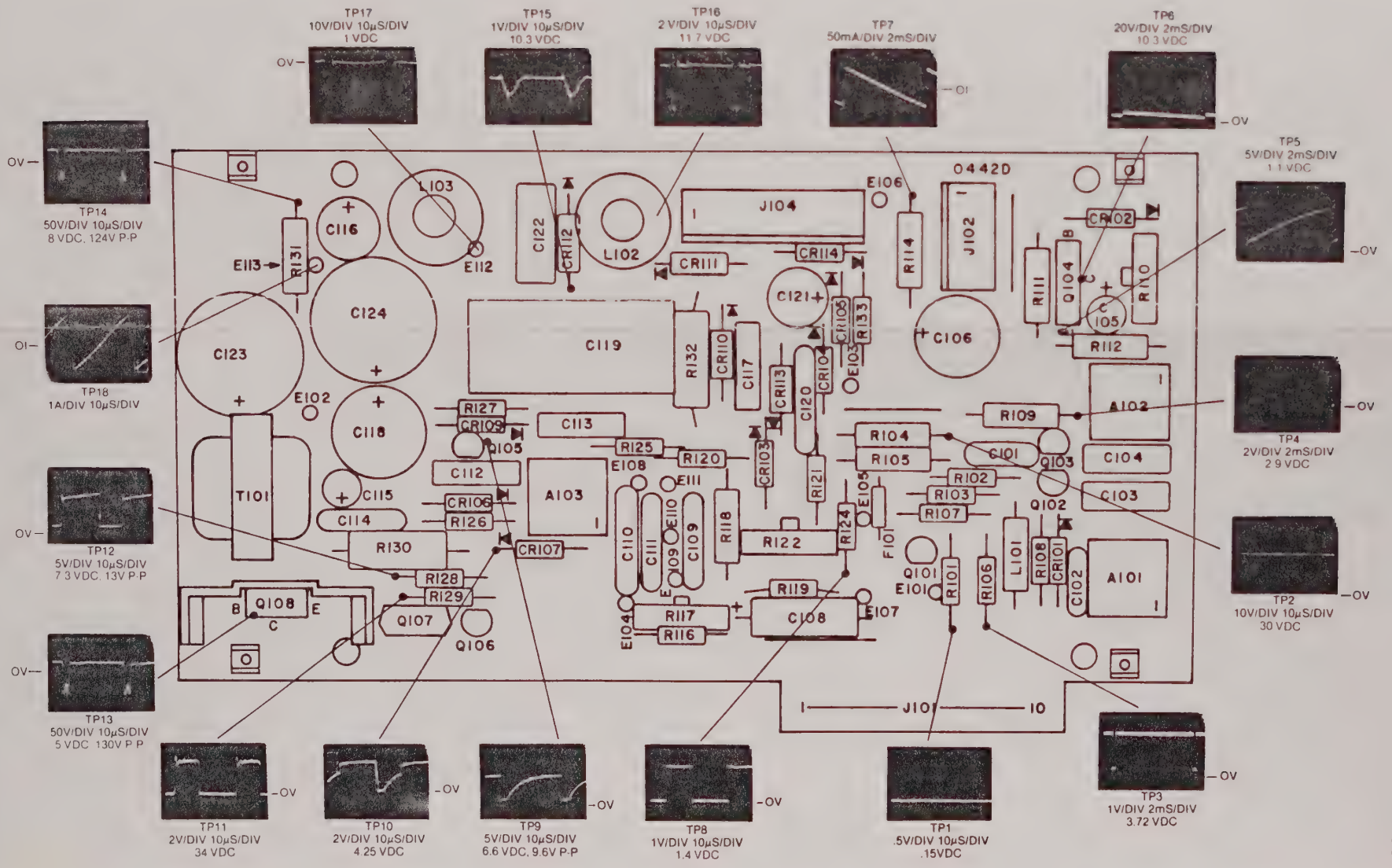
	SIGNATURE	DATE	SIZE	DRAWING NO	DEV
DRAFTSMAN	Gregory L. Cook	7-21-77	D	1-024-0590	B
CHECKER	M Lundgren	8-26-77			
DESIGNER			USED ON	SCALE: NONE	SHEET: 1 of 1
ENGINEER	W. Baller	8/26/77			

PARTS LIST TV50

REF SYM	DESCRIPTION	BBRC PART NUMBER	USED ON 6-002- 0689	0732
A101	RES TRIM, 60K, VERT HOLD	1-011-8006	X	X
A102	RES TRIM, 20K, VERT LIN	1-011-8005	X	X
A103	RES TRIM, 2.5K, VIDEO CENTER	1-011-8001	X	X
	CAPACITOR, FIXED, uF UNLESS NOTED			
C101	100pF±5%, 500V, DM	1-012-0300	X	X
C102	.005±20%; 100V, CD	10-12-7508	X	X
C103	.22±10%; 100V, MY	1-012-2277	X	X
C104	.22±10%; 100V, MY	1-012-2277	X	X
C105	.68; 50V, E	1-012-2264	X	X
C106	470; 10V, E	1-012-2158	X	X
C107	NOT USED			
C108	25; 25V, E	1-012-1380	X	X
C109	.01±20%; 1000V, CD	1-012-2214	X	X
C110	.02±20%; 1000V, CD	1-012-2217	X	X
C111	.01±20%; 1000V, CD	1-012-2214	X	X
C112	.0022±10%; 630V, MY	1-012-2254	X	X
C113	.0047±10%; 630V, MY	1-012-2279	X	X
C114	.02±20%; 100V, CD	10-12-7209	X	X
C115	1; 50V, E	1-012-2189	X	X
C116	50; 50V, E	1-012-2157	X	X
C117	.047±10%; 250V, MY	1-012-2240	X	X
C118	220; 25V, E	1-012-2159	X	X
C119	10±10%; 100V, MY	1-012-2255	X	X
C120	.02±20%; 500V, CD	1-012-0780	X	X
C121	50; 50V, E	1-012-2157	X	X
C122	.022±10%; 250V, PP	1-012-2297	X	X
C123	10-25V, E	1-012-2273	X	X
C124	10; 25V, E	1-012-2273	X	X
	DIODE			
CR1	H510	1-021-0424	X	X
CR101	1N3605	1-021-0410	X	X
CR102	1N3605	1-021-0410	X	X
CR103	1N3605	1-021-0410	X	X
CR104	1N3605	1-021-0410	X	X
CR105	1N3605	1-021-0410	X	X
CR106	1N3605	1-021-0410	X	X
CR107	1N3605	1-021-0410	X	X
CR108	NOT USED			
CR109	1N3605	1-021-0410	X	X
CR110	1N3280/B599	1-021-0403	X	X
CR111	30S3	1-021-0458	X	X
CR112	30S3	1-021-0458	X	X
CR113	1N3280/B599	1-021-0403	X	X
CR114	1N3605	1-021-0410	X	X
	FUSE			
F101	2A-125V, PICO	1-028-0247	X	X
	CONNECTORS			
J102	CONNECTOR, 4 PIN MALE	1-039-0146	X	X
J103	NOT USED			
J104	CONNECTOR, 7 PIN MALE	1-039-0145	X	X

REF SYM	DESCRIPTION	BBRC PART NUMBER	USED ON 6-002- 0698	0732
L1	VERTICAL CHOKE	6-003-0529	X	X
L2	DEFLECTION, TV50	1-023-0231	X	X
L101	560uH	1-016-0302	X	X
L102	LINEARITY	1-016-0328	X	X
L103	WIDTH	1-016-0303	X	X
	TRANSISTOR			
Q101	2N5830	1-015-1172	X	X
Q102	2N6027	1-015-1157	X	X
Q103	MPS-A65	1-015-1186	X	X
Q104	MJE3055	1-015-1156	X	X
Q105	2N4124	1-015-1139	X	X
Q106	2N4124	1-015-1139	X	X
Q107	MPS-U05	1-015-1159	X	X
Q108	BU407	1-015-1210	X	X
	RESISTOR, FIXED, CARBON, ±5%; 1/4W UNLESS NOTED			
R101	47	70-16-0470	X	X
R102	100	70-16-0101	X	X
R103	47	70-16-0470	X	X
R104	220; 1/2W	1-011-2254	X	X
R105	820; 1/2W	1-011-2268	X	X
R106	470	70-16-0471	X	X
R107	360	70-16-0361	X	X
R108	100K	70-16-0104	X	X
R109	180	1-011-2252	X	X
R110	VAR; 250±20%; CO VERT HGT	70-89-0251	X	X
R111	12; 1/2W	1-011-2224	X	X
R112	15; 1/2W	1-011-2226	X	X
R113	NOT USED			
R114	1.5K; 1/2W	1-011-2274	X	X
R115	NOT USED			
R116	62K	70-16-0623	X	X
R117	VAR; 100K±20%; CO BRT ADJ	1-011-5435	X	
R118	30K; 1/2W	1-011-2305	X	X
R119	9.1K	70-16-0912	X	X
R120	8.2M	70-16-0825	X	X
R121	100K	70-16-0104	X	X
R122	VAR; 2.5M±20%, CO FOC ADJ	1-011-5566	X	X
R123	NOT USED			
R124	510	70-16-0511	X	X
R125	1K	70-16-0102	X	X
R126	20K	70-16-0203	X	X
R127	3.3K	70-16-0332	X	X
R128	15K	70-16-0153	X	X
R129	2.4K	70-16-0242	X	X
R130	82±10%; 3W, WW	1-011-2375	X	X
R131	3; 1/2W	1-011-2478	X	X
R132	1.2±10%; 2W, WW	1-011-1395	X	X
R133	6.8K	70-16-0682	X	X
R134	NOT USED			
R135	NOT USED			
	TRANSFORMER			
T1	NOT USED			
T2	HIGH VOLTAGE	6-003-0587	X	X
T101	HORIZ DRIVER	1-017-5402	X	X
	MISCELLANEOUS			
	CRT SOCKET	1-022-0427	X	X

Figure 6-2 TV50 Parts List, Waveform, and Component Layout


TP17
10V/DIV 10µS/DIV
1 VDC
TP15
1V/DIV 10µS/DIV
10.3 VDC
TP16
2 V/DIV 10µS/DIV
11.7 VDC
TP7
50mA/DIV 2mS/DIV
TP6
20V/DIV 2mS/DIV
10.3 VDC
TP5
5V/DIV 2mS/DIV
1.1 VDC
TP14
50V/DIV 10µS/DIV
8 VDC, 124V P-P
TP18
1A/DIV 10µS/DIV
TP12
5V/DIV 10µS/DIV
7.3 VDC, 13V P-P
TP13
50V/DIV 10µS/DIV
5 VDC 130V P-P
TP4
2V/DIV 2mS/DIV
2.9 VDC
TP2
10V/DIV 10µS/DIV
30 VDC
TP11
2V/DIV 10µS/DIV
34 VDC
TP10
2V/DIV 10µS/DIV
4.25 VDC
TP9
5V/DIV 10µS/DIV
6.6 VDC, 9.6V P-P
TP8
1V/DIV 10µS/DIV
1.4 VDC
TP1
.5V/DIV 10µS/DIV
.15VDC
TP3
1V/DIV 2mS/DIV
3.72 VDC
0442D
J104
J102
J101
L103
L102
C116
C122
C124
C123
C119
C121
C106
C118
C115
C114
C113
C112
C120
C117
C110
C111
C109
C108
C107
C105
C104
C103
C102
A103
A102
A101
T101
R131
R130
R132
R133
R125
R120
R127
R126
R128
R129
R122
R124
R121
R118
R119
R117
R116
R114
R111
R110
R112
R109
R104
R105
R102
R103
R107
R108
R106
R101
CR114
CR111
CR112
CR113
CR110
CR109
CR108
CR107
CR106
CR105
CR104
CR103
CR102
CR101
Q108
Q107
Q106
Q105
Q104
Q103
Q102
Q101
F101
E101
E102
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E109
E110
E111
E112
E113
OV
OI
IO

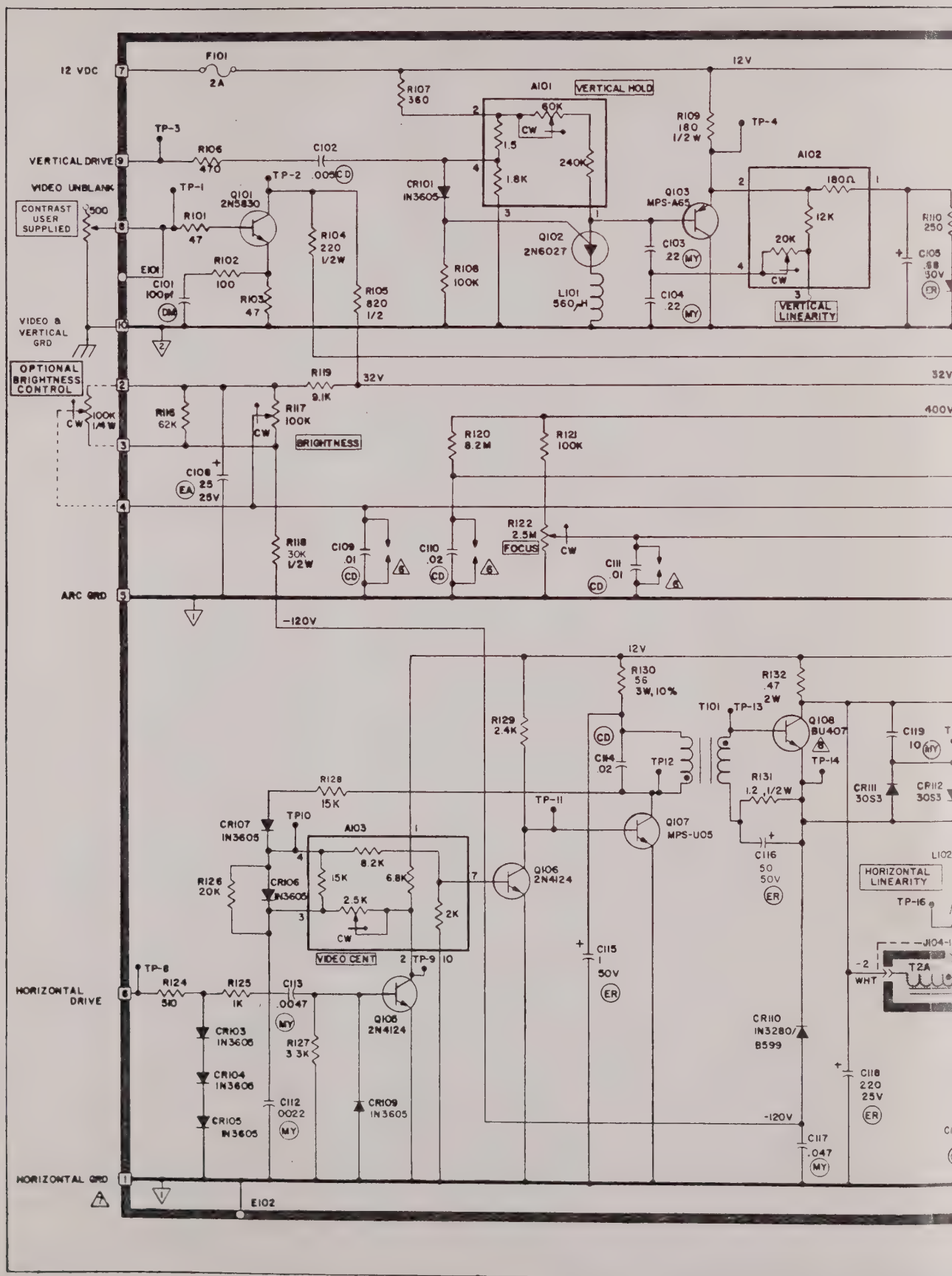
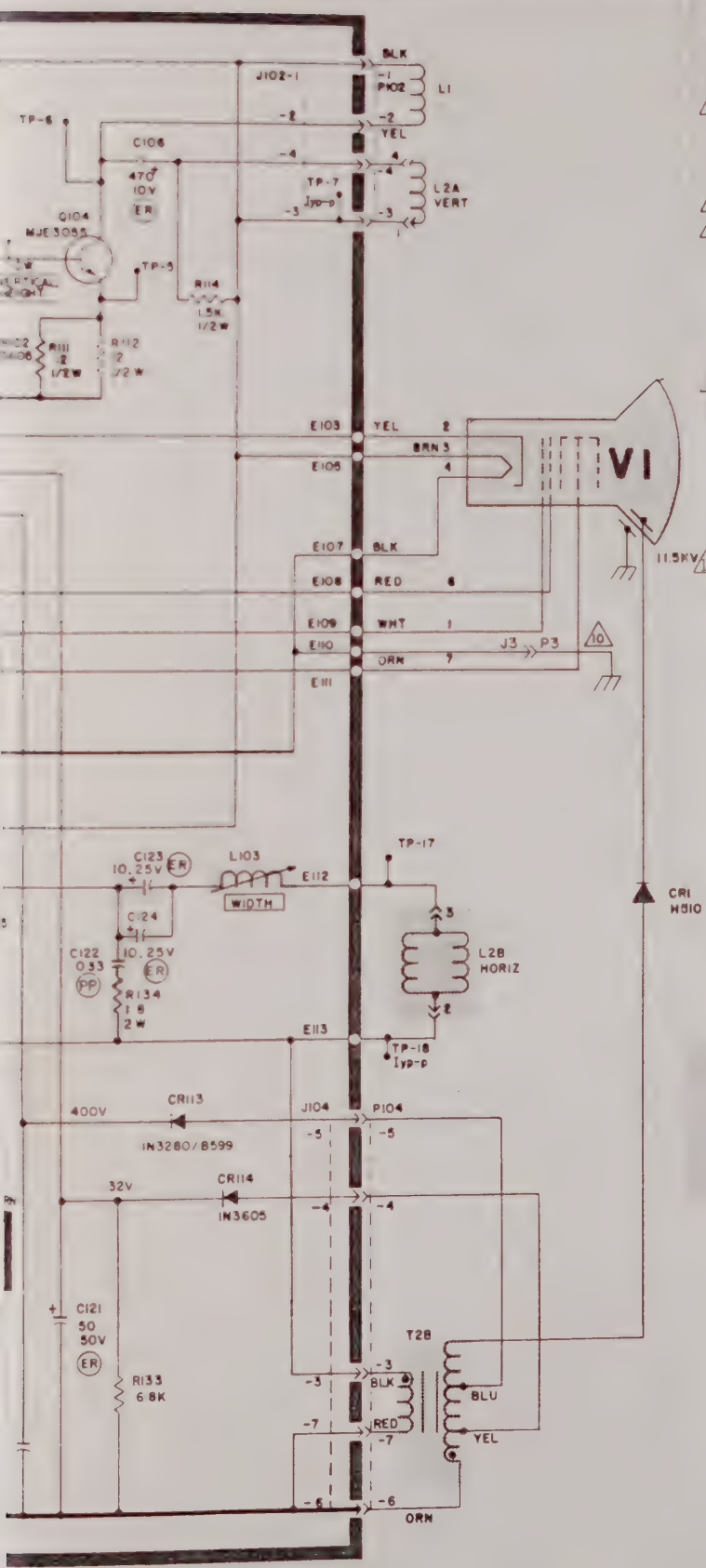


Figure 6-3 TV 90/120



GENERAL NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS 1/4W, 5%, VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS. FOR CAPACITOR TYPES, SEE NOTE #9.
3. □ DENOTES J101 PC CARD EDGE CONNECTOR.
4. →)→ DENOTES CONNECTION TO OFF BOARD COMPONENTS.
5. REFERENCE DESIGNATIONS NOT USED: R113, R115
   LAST REFERENCE DESIGNATION USED: R134, C124
6. PROTECTIVE ARC GAPS ARE AN INTEGRAL PART OF PRINTED WIRE BOARD.
7. THE PWB CIRCUIT GROUNDS ARE BROUGHT OUT SEPARATELY TO PINS 1, 5 AND 10 OF J101. PWB CIRCUIT GROUNDS FOR PINS 1 AND 5 OF J101 ARE CONNECTED TOGETHER BY A JUMPER WIRE ON THE BOARD AND ARE CONNECTED TO CHASSIS GROUND VIA A WIRE FROM E110.

   THE DATA DISPLAY UNIT IS CONNECTED TO THE SYSTEM GROUND THROUGH PINS 1 AND 10 OF J101. FOR NON-STANDARD GROUNDING TECHNIQUES REFER TO SECTION 2 OF THE SERVICE MANUAL.
8. DENOTES HEATSINK
9. (DM) = DIPPED MICA
   (CD) = CERAMIC DISC.
   (MY) = MYLAR
   (EA) = ELECTROLYTIC AXIAL
   (ER) ELECTROLYTIC RADIAL
   (PP) = POLYPROPYLENE
10. P3 AND J3 ARE USED ONLY ON THE TVX90 AND TVX120 MODELS.

PRODUCT SAFETY MUST BE CONSIDERED WHEN ANY COMPONENT IS REPLACED IN THIS MONITOR. THE CRITICAL COMPONENTS THAT AFFECT X-RADIATION ARE DENOTED IN THE SHADED AREAS ON THE SCHEMATIC. COMPONENTS IN THE SHADED AREA ARE TO BE REPLACED ONLY WITH EDO DIV. APPROVED COMPONENTS.

THE USE OF SUBSTITUTE COMPONENTS WHICH DO NOT HAVE THE SAME CHARACTERISTICS AS THE EDO DIV. ORIGINAL COMPONENTS MAY CREATE EXCESSIVE X-RADIATION.

	SIGNATURE	DATE
DRAFTSMAN		
CHECKER		8-2-77
DESIGNER		
ENGINEER	W. Bak	

TITLE: SCHEMATIC
TV-90/120 DC
12 VOLT

SIZE	DRAWING NO	REV
D	1-024-0584	B

USED ON

SCALE: NONE

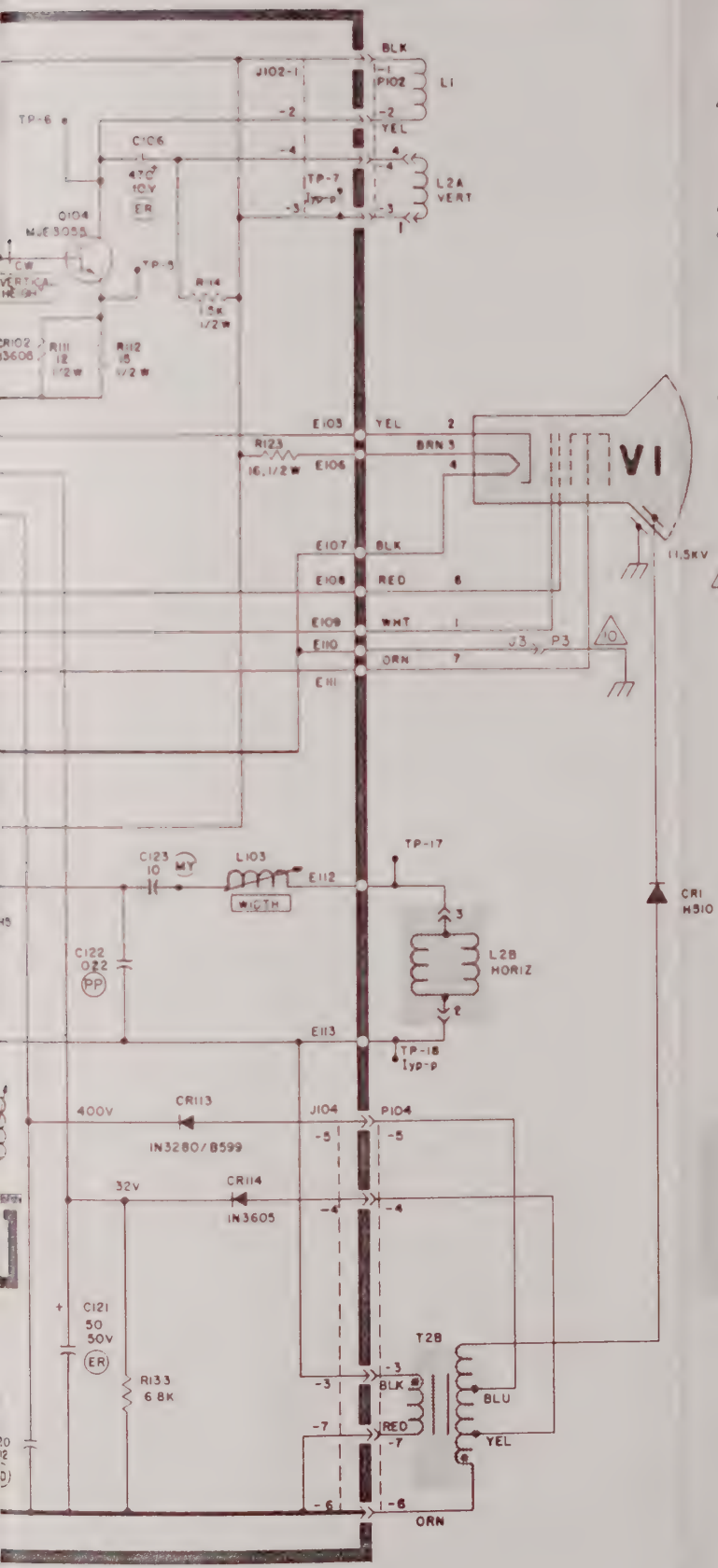
SHEET 1 OF 2

PARTS LIST TV 90/120, 12V

REF SYM	DESCRIPTION	BBRC PART NUMBER	USED ON 6-002 0698	0686	0697	0710	0733	0731	0735
A101	RES TRIM, 60K, VERT HOLD	1-011-8006	X	X	X	X	X	X	X
A102	RES TRIM, 20K, VERT LIN	1-011-8005	X	X	X	X	X	X	X
A103	RES TRIM, 2.5K, VIDEO CENTER	1-011-8001	X	X	X	X	X	X	X
	CAPACITOR, FIXED, uF UNLESS NOTED								
C101	100pF±5%, 500v, DM	1-012-0300	X	X	X	X	X	X	X
C102	.005±20%; 100v, CD	10-12-7508	X	X	X	X	X	X	X
C103	.22±10%; 100v, MY	1-012-2277	X	X	X	X	X	X	X
C104	.22±10%; 100v, MY	1-012-2277	X	X	X	X	X	X	X
C105	.68; 50v, E	1-012-2264	X	X	X	X	X	X	X
C106	470; 10v, E	1-012-2158	X	X	X	X	X	X	X
C107	NOT USED								
C108	25; 25v, E	1-012-1380	X	X	X	X	X	X	X
C109	.01±20%; 1000v, CD	1-012-2214	X	X	X	X	X	X	X
C110	.02±20%; 1000v, CD	1-012-2217	X	X	X	X	X	X	X
C111	.01±20%; 1000v, CD	1-012-2214	X	X	X	X	X	X	X
C112	.0022±10%; 630v, MY	1-012-2254	X	X	X	X	X	X	X
C113	.0047±10%; 630v, MY	1-012-2279	X	X	X	X	X	X	X
C114	.02±20%; 100v, CD	10-12-7209	X	X	X	X	X	X	X
C115	1; 50v, E	1-012-2189	X	X	X	X	X	X	X
C116	50; 50v, E	1-012-2157	X	X	X	X	X	X	X
C117	.047±10%; 250v, MY	1-012-2240	X	X	X	X	X	X	X
C118	220; 25v, E	1-012-2159	X	X	X	X	X	X	X
C119	10±10%; 100v, MY	1-012-2255	X	X	X	X	X	X	X
C120	.02±20%; 500v, CD	1-012-0780	X	X	X	X	X	X	X
C121	50; 50v, E	1-012-2157	X	X	X	X	X	X	X
C122	.033±10%; 250V, MY	1-012-2298	X	X	X	X	X	X	X
C123	10; 25v, E	1-012-2273	X	X	X	X	X	X	X
C124	10; 25v, E	1-012-2273	X	X	X	X	X	X	X
	DIODE								
CR1	H510	1-021-0424	X	X	X	X	X	X	X
CR101	1N3605	1-021-0410	X	X	X	X	X	X	X
CR102	1N3605	1-021-0410	X	X	X	X	X	X	X
CR103	1N3605	1-021-0410	X	X	X	X	X	X	X
CR104	1N3605	1-021-0410	X	X	X	X	X	X	X
CR105	1N3605	1-021-0410	X	X	X	X	X	X	X
CR106	1N3605	1-021-0410	X	X	X	X	X	X	X
CR107	1N3605	1-021-0410	X	X	X	X	X	X	X
CR108									
CR109	1N3605	1-021-0410	X	X	X	X	X	X	X
CR110	1N3280/B599	1-021-0403	X	X	X	X	X	X	X
CR111	30S3	1-021-0458	X	X	X	X	X	X	X
CR112	30S3	1-021-0458	X	X	X	X	X	X	X
CR113	1N3280/B599	1-021-0403	X	X	X	X	X	X	X
CR114	1N3605	1-021-0410	X	X	X	X	X	X	X
	FUSE								
F101	2A-125v, PICO	1-028-0247	X	X	X	X	X	X	X
	CONNECTORS								
J102	CONNECTOR, 4 PIN MALE	1-039-0146	X	X	X	X	X	X	X
J103	NOT USED								
J104	CONNECTOR, 7 PIN MALE	1-039-0145	X	X	X	X	X	X	X
P3	CONNECTOR, 1 PIN FEMALE	1-034-0323				X			X
J3	CONNECTOR, 1 PIN MALE	1-034-0300				X			X
	COIL								
L1	VERTICAL CHOKE	6-003-0572	X	X	X	X	X	X	X
L2	DEFLECTION, TV 120	1-023-0239			X	X	X		X
	OR DEFLECTION, TV 90	1-023-0240	X	X				X	
L101	560uH	1-016-0302	X	X	X	X	X	X	X
L102	LINEARITY	1-016-0328	X	X	X	X	X	X	X
L103	WIDTH	1-016-0323	X	X	X	X	X	X	X

REF SYM	DESCRIPTION	BBRC PART NUMBER	USED ON 0698	06
	TRANSISTOR			
Q101	2N5830	1-015-1172	X	
Q102	2N6027	1-015-1157	X	
Q103	MPS-A65	1-015-1186	X	
Q104	MJE3055	1-015-1156	X	
Q105	2N4124	1-015-1139	X	
Q106	2N4124	1-015-1139	X	
Q107	MPS-U05	1-015-1159	X	
Q108	BU407	1-015-1210	X	
	RESISTOR, FIXED, CARBON, ±5%; 1/4w UNLESS NOTED			
R101	47	70-16-0470	X	
R102	100	70-16-0101	X	
R103	47	70-16-0470	X	
R104	220; 1/2w	1-011-2254	X	
R105	820; 1/2w	1-011-2268	X	
R106	470	70-16-0471	X	
R107	360	70-16-0361	X	
R108	100K	70-16-0104	X	
R109	180	1-011-2252	X	
R110	VAR; 250±20%; CO VERT HGT	70-89-0251	X	
R111	12; 1/2w	1-011-2224	X	
R112	12; 1/2w	1-011-2224	X	
R113	NOT USED			
R114	1.5K; 1/2w	1-011-2274	X	
R115	NOT USED			
R116	62K	70-16-0623	X	
R117	VAR; 100K±20%; CO BRT ADJ	1-011-5435	X	
R118	30K; 1/2w	1-011-2305	X	
R119	9.1K	70-16-0912	X	
R120	8.2M	70-16-0825	X	
R121	100K	70-16-0104	X	
R122	VAR: 2.5M±20%, CO FOC ADJ	1-011-5566	X	
R123	NOT USED			
R124	510	70-16-0511	X	
R125	1K	70-16-0102	X	
R126	20K	70-16-0203	X	
R127	3.3K	70-16-0332	X	
R128	15K	70-16-0153	X	
R129	2.4K	70-16-0242	X	
R130	56±10%; 3W, WW	70-16-2521	X	
R131	1.2; 1/2w	1-011-2520	X	
R132	.47±10%; 2w, WW	1-011-1394	X	
R133	6.8K	70-16-0682	X	
R134	1.8±5%; 2W	1-011-2417	X	
R135	NOT USED			
	TRANSFORMER			
T1	NOT USED			
T2	HIGH VOLTAGE, TV90	6-003-0605	X	
	OR HIGH VOLTAGE, TV90/TRW	6-003-0571		
	OR HIGH VOLTAGE, TV120	6-003-0599		
	OR HIGH VOLTAGE, TVX120	6-003-0586		
T101	HORIZ DRIVER	1-017-5402	X	
	MISCELLANEOUS			
	CRT SOCKET	1-022-0427	X	

Figure 6-4 TV 90/120, 12V Parts List, Waveform and Component Layout



GENERAL NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS 1/4W, 5%, VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS. FOR CAPACITOR TYPES, SEE NOTE #9.
3. ⟦ ⟧ DENOTES J101 PC CARD EDGE CONNECTOR.
4. >> DENOTES CONNECTION TO OFF BOARD COMPONENTS.
5. REFERENCE DESIGNATIONS NOT USED: R113, R115
   LAST REFERENCE DESIGNATION USED: R133, C123
6. PROTECTIVE ARC GAPS AN INTEGRAL PART OF THE PRINTED WIRE BOARD.
7. THE PWB CIRCUIT GROUNDS ARE BROUGHT OUT SEPARATELY TO PINS 1, 5 AND 10 OF J101. PWB CIRCUIT GROUNDS FOR PINS 1 AND 5 OF J101 ARE CONNECTED TOGETHER BY A JUMPER WIRE ON THE BOARD AND ARE CONNECTED TO CHASSIS GROUND VIA A WIRE FROM E110.

   THE DATA DISPLAY UNIT IS CONNECTED TO THE SYSTEM GROUND THROUGH PINS 1 AND 10 OF J101. FOR NON-STANDARD GROUNDING TECHNIQUES REFER TO SECTION 2 OF THE SERVICE MANUAL.
8. DENOTES HEATSINK
9. (DM) = DIPPED MICA
   (CD) = CERAMIC DISC.
   (MY) = MYLAR
   (EA) = ELECTROLYTIC AXIAL
   (ER) = ELECTROLYTIC RADIAL
   (PP) = POLYPROPYLENE
10. P3 AND J3 ARE USED ONLY ON THE TVX90 AND TVX120 MODELS.

PRODUCT SAFETY MUST BE CONSIDERED WHEN ANY COMPONENT IS REPLACED IN THIS MONITOR. THE CRITICAL COMPONENTS THAT AFFECT X-RADIATION ARE DENOTED IN THE SHADED AREAS ON THE SCHEMATIC. COMPONENTS IN THE SHADED AREA ARE TO BE REPLACED ONLY WITH EDD DIV. APPROVED COMPONENTS.

THE USE OF SUBSTITUTE COMPONENTS WHICH DO NOT HAVE THE SAME CHARACTERISTICS AS THE EDD DIV. ORIGINAL COMPONENTS MAY CREATE EXCESSIVE X-RADIATION.

	SIGNATURE	DATE
DRAFTSMAN		
CHECKER		
DESIGNER		
ENGINEER		

TITLE: SCHEMATIC
TV 90/120DC
15 VOLT

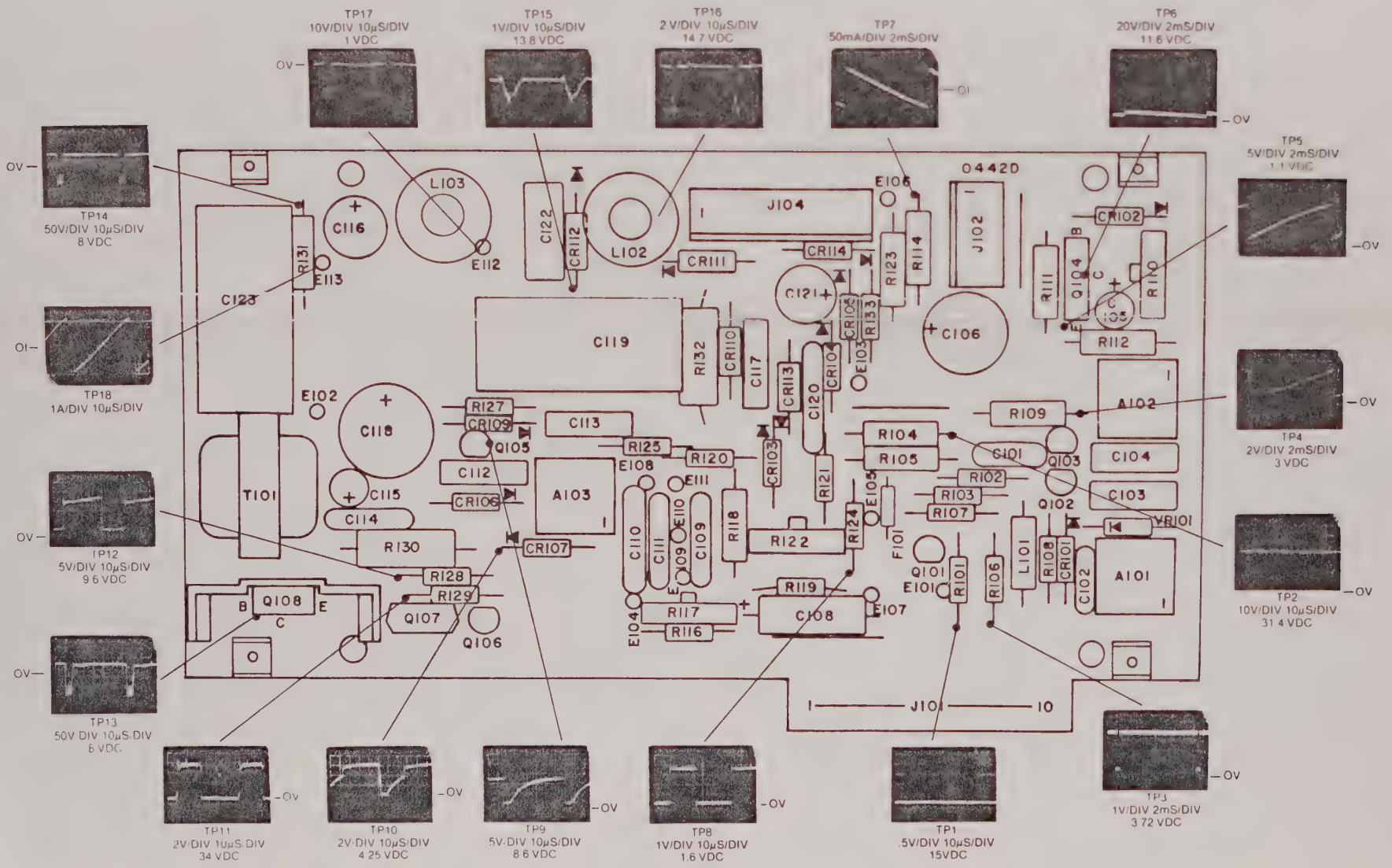
SIZE: D | DRAWING NO: 1-024-0589 | REV: B
USED ON | SCALE: NONE | SHEET: 1 OF 2

PARTS LIST TV 90/120, 15V

REF SYM	DESCRIPTION	BBRC PART NUMBER	USED ON 6-002- 0695	0688	0713	0728	0730	0734
A101	RES TRIM, 60K, VERT HOLD	1-011-8006	X	X	X	X	X	X
A102	RES TRIM, 20K, VERT LIN	1-011-8005	X	X	X	X	X	X
A103	RES TRIM, 2.5K, VIDEO CENTER	1-011-8001	X	X	X	X	X	X
	CAPACITOR, FIXED, uF UNLESS NOTED							
C101	100PF±5%, 500V, DM	1-012-0300	X	X	X	X	X	X
C102	.005±20%; 100V, CD	10-12-7508	X	X	X	X	X	X
C103	.22±10%; 100V, MY	1-012-2277	X	X	X	X	X	X
C104	.22±10%; 100V, MY	1-012-2277	X	X	X	X	X	X
C105	.68; 50V, E	1-012-2264	X	X	X	X	X	X
C106	470; 10V, E	1-012-2158	X	X	X	X	X	X
C107	NOT USED							
C108	25; 25V, E	1-012-1380	X	X	X	X	X	X
C109	.01±20%; 1000V, CD	1-012-2214	X	X	X	X	X	X
C110	.02±20%; 1000V, CD	1-012-2217	X	X	X	X	X	X
C111	.01±20%; 1000V, CD	1-012-2214	X	X	X	X	X	X
C112	.022±10%; 630V, MY	1-012-2254	X	X	X	X	X	X
C113	.0047±10%; 630V, MY	1-012-2279	X	X	X	X	X	X
C114	.02±20%; 100V, CD	10-12-7209	X	X	X	X	X	X
C115	1; 50V, E	1-012-2189	X	X	X	X	X	X
C116	50; 50V, E	1-012-2157	X	X	X	X	X	X
C117	.047±10%; 250V, MY	1-012-2240	X	X	X	X	X	X
C118	220; 25V, E	1-012-2159	X	X	X	X	X	X
C119	10±10%; 100V, MY	1-012-2255	X	X	X	X	X	X
C120	.02±20%; 500V, CD	1-012-0780	X	X	X	X	X	X
C121	50; 50V, E	1-012-2157	X	X	X	X	X	X
C122	.022±10%; 250V, PP	1-012-2297	X	X	X	X	X	X
C123	10±10%; 100V, MY	1-012-2255	X	X	X	X	X	X
C124	NOT USED							
	DIODE							
CR1	H510	1-021-0424	X	X	X	X	X	X
CR101	1N3605	1-021-0410	X	X	X	X	X	X
CR102	1N3605	1-021-0410	X	X	X	X	X	X
CR103	1N3605	1-021-0410	X	X	X	X	X	X
CR104	1N3605	1-021-0410	X	X	X	X	X	X
CR105	1N3605	1-021-0410	X	X	X	X	X	X
CR106	1N3605	1-021-0410	X	X	X	X	X	X
CR107	1N3605	1-012-0410	X	X	X	X	X	X
CR108	NOT USED							
CR109	1N3605	1-021-0410	X	X	X	X	X	X
CR110	1N3280/B599	1-021-0403	X	X	X	X	X	X
CR111	30S3	1-021-0458	X	X	X	X	X	X
CR112	30S3	1-021-0458	X	X	X	X	X	X
CR113	1N3280/B599	1-021-0403	X	X	X	X	X	X
CR114	1N3605	1-021-0410	X	X	X	X	X	X
	FUSE							
F101	2A-125V, PICO	1-028-0247	X	X	X	X	X	X
	CONNECTORS							
J102	CONNECTOR, 4 PIN MALE	1-039-0146	X	X	X	X	X	X
J103	NOT USED							
J104	CONNECTOR, 7 PIN MALE	1-039-0145	X	X	X	X	X	X
P3	CONNECTOR, 1 PIN FEMALE	1-034-0323				X		X
J3	CONNECTOR, 1 PIN MALE	1-034-0300				X		X
	COIL							
L1	VERTICAL CHOKE	6-003-0529	X	X	X	X	X	X
L2	DEFLECTION TV90	1-023-0237	X				X	
	OR DEFLECTION TVX 120/TV120	1-023-0231		X	X	X		X
L101	560uH	1-016-0302	X	X	X	X	X	X
L102	LINEARITY	1-016-0328	X	X	X	X	X	X
L103	WIDTH	1-016-0323	X	X	X	X	X	X

REF SYM	DESCRIPTION	BBRC PART NUMBER	USED ON 6 0695	0688
	TRANSISTOR			
Q101	2N5830	1-015-1172	X	X
Q102	2N6027	1-015-1157	X	X
Q103	MPS-A65	1-015-1186	X	X
Q104	MJE3055	1-015-1156	X	X
Q105	2N4124	1-015-1139	X	X
Q106	2N4124	1-015-1139	X	X
Q107	MPS-U05	1-015-1159	X	X
Q108	BU407	1-015-1210	X	X
	RESISTOR, FIXED, CARBON, ±5%; 1/4W UNLESS NOTED			
R101	47	70-16-0470	X	X
R102	100	70-16-0101	X	X
R103	47	70-16-0470	X	X
R104	220; 1/2W	1-011-2254	X	X
R105	820; 1/2W	1-011-2268	X	X
R106	470	70-16-0471	X	X
R108	100K	70-16-0104	X	X
R109	300; 1/2W	1-011-2257	X	X
R110	VAR: 250±20%; CO VERT HGT	70-89-0251	X	X
R111	12; 1/2W	1-011-2224	X	X
R112	15; 1/2W	1-011-2226	X	X
R113	NOT USED			
R114	1/5K 1/2W	1-011 2274	X	X
R115	NOT USED			
R116	62K	70-16-0623	X	X
R117	VAR; 100K±20%; CO BRT ADJ	1-011-5435	X	X
R118	30K; 1/2W	1-011-2305	X	X
R119	9.1K	70-16-0912	X	X
R120	8.2M	70-16-0825	X	X
R121	100K	70-16-0104	X	X
R122	VAR; 2.5M±20%, CO FOC ADJ	1-011-5566	X	X
R123	16; 1/2W	1-011-2227	X	X
R124	510	70-16-0511	X	X
R125	1K	70-16-0102	X	X
R126	NOT USED			
R127	3.3K	70-16-0332	X	X
R128	15K	70-16-0153	X	X
R129	3K	70-16-0302	X	X
R130	82±10%; 3W, WW	1-011-2375	X	X
R131	3; 1/2W, CO	1-011-2478	X	X
R132	1.2±10%; 2W, WW	1-011-1395	X	X
R133	6.8K	70-16-0682	X	X
R134	NOT USED			
	TRANSISTOR			
T1	NOT USED			
T2	HIGH VOLTAGE TV90/15V	6-003-0602	X	
	OR HIGH VOLTAGE TV120/15V	6-003-0530		X
	OR HIGH VOLTAGE TV120	6-003-0587		
	OR HIGH VOLTAGE TVX120	6-003-0604		
T101	HORIZ DRIVER	1-017-5402	X	X
	MISCELLANEOUS			
	CRT SOCKET	1-022-0427	X	X

Figure 6-6 TV 90/120, 15V Parts List, Waveform and Component Layout


TP17
10V/DIV 10µS/DIV
1 VDC
TP15
1V/DIV 10µS/DIV
13.8 VDC
TP16
2 V/DIV 10µS/DIV
14.7 VDC
TP7
50mA/DIV 2mS/DIV
TP6
20V/DIV 2mS/DIV
11.6 VDC
TP5
5V/DIV 2mS/DIV
1.1 VDC
TP14
50V/DIV 10µS/DIV
8 VDC
TP18
1A/DIV 10µS/DIV
TP12
5V/DIV 10µS/DIV
9.6 VDC
TP13
50V DIV 10µS/DIV
6 VDC
TP4
2V/DIV 2mS/DIV
3 VDC
TP2
10V/DIV 10µS/DIV
31.4 VDC
TP11
2V/DIV 10µS/DIV
34 VDC
TP10
2V/DIV 10µS/DIV
4.25 VDC
TP9
5V/DIV 10µS/DIV
8.6 VDC
TP8
1V/DIV 10µS/DIV
1.6 VDC
TP1
.5V/DIV 10µS/DIV
15VDC
TP3
1V/DIV 2mS/DIV
3.72 VDC
0442D
J104
J102
J101
A101
A102
A103
L103
L102
T101
C116
C123
C122
C112
C119
C121
C106
C118
C115
C114
C113
C120
C117
C110
C111
C109
C108
C107
C104
C103
C102
R131
R130
R128
R129
R127
R125
R120
R121
R122
R124
R119
R117
R116
R118
R132
R123
R114
R111
R110
R112
R109
R104
R105
R102
R103
R107
R101
R106
R108
Q108
Q107
Q106
Q105
Q104
Q103
Q102
Q101
CR102
CR114
CR111
CR110
CR113
CR103
CR109
CR106
CR107
CR101
VR101
F101
E113
E112
E102
E108
E111
E110
E109
E104
E105
E106
E103
E107
OV
OI
10

IM1035

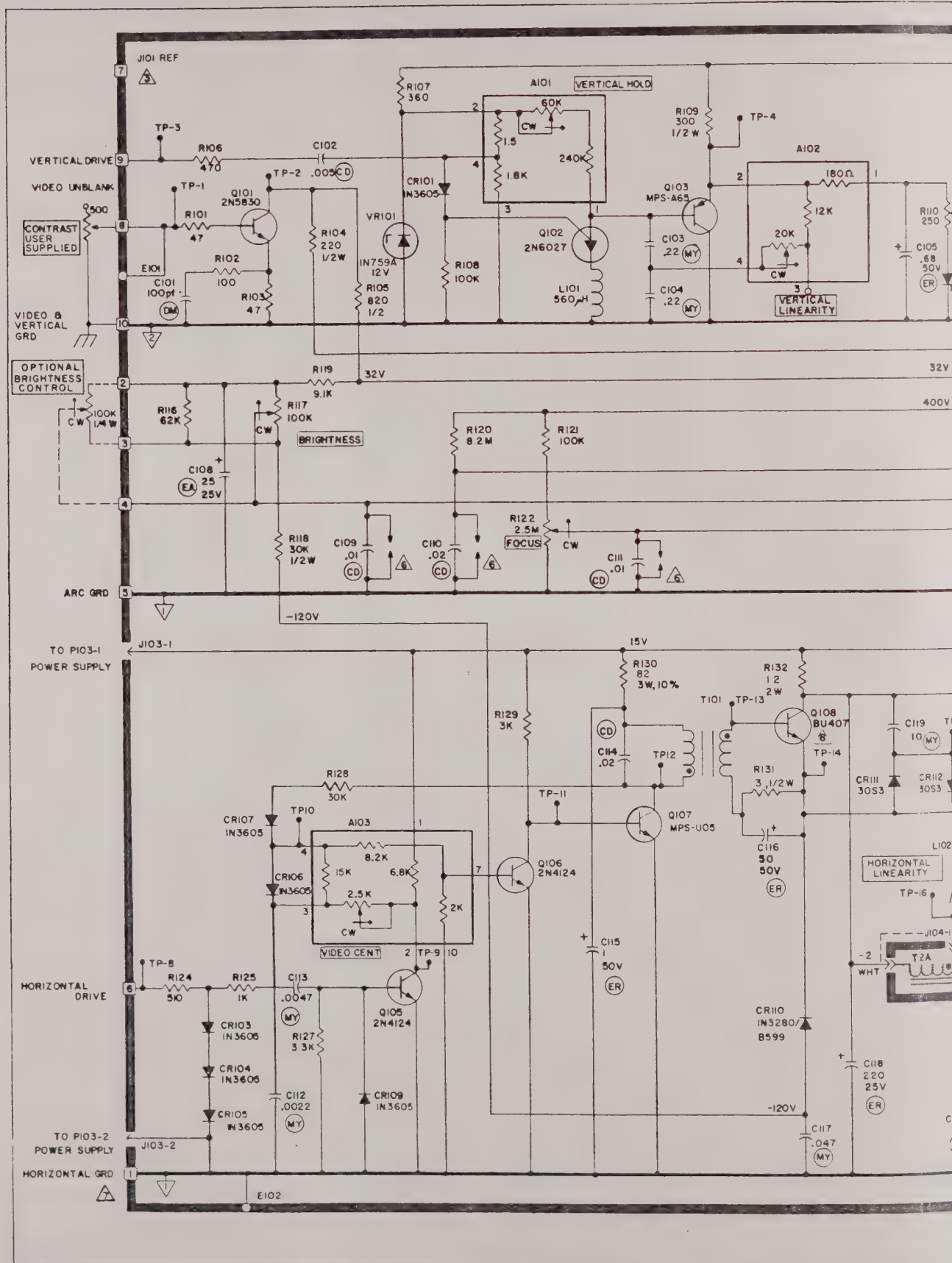
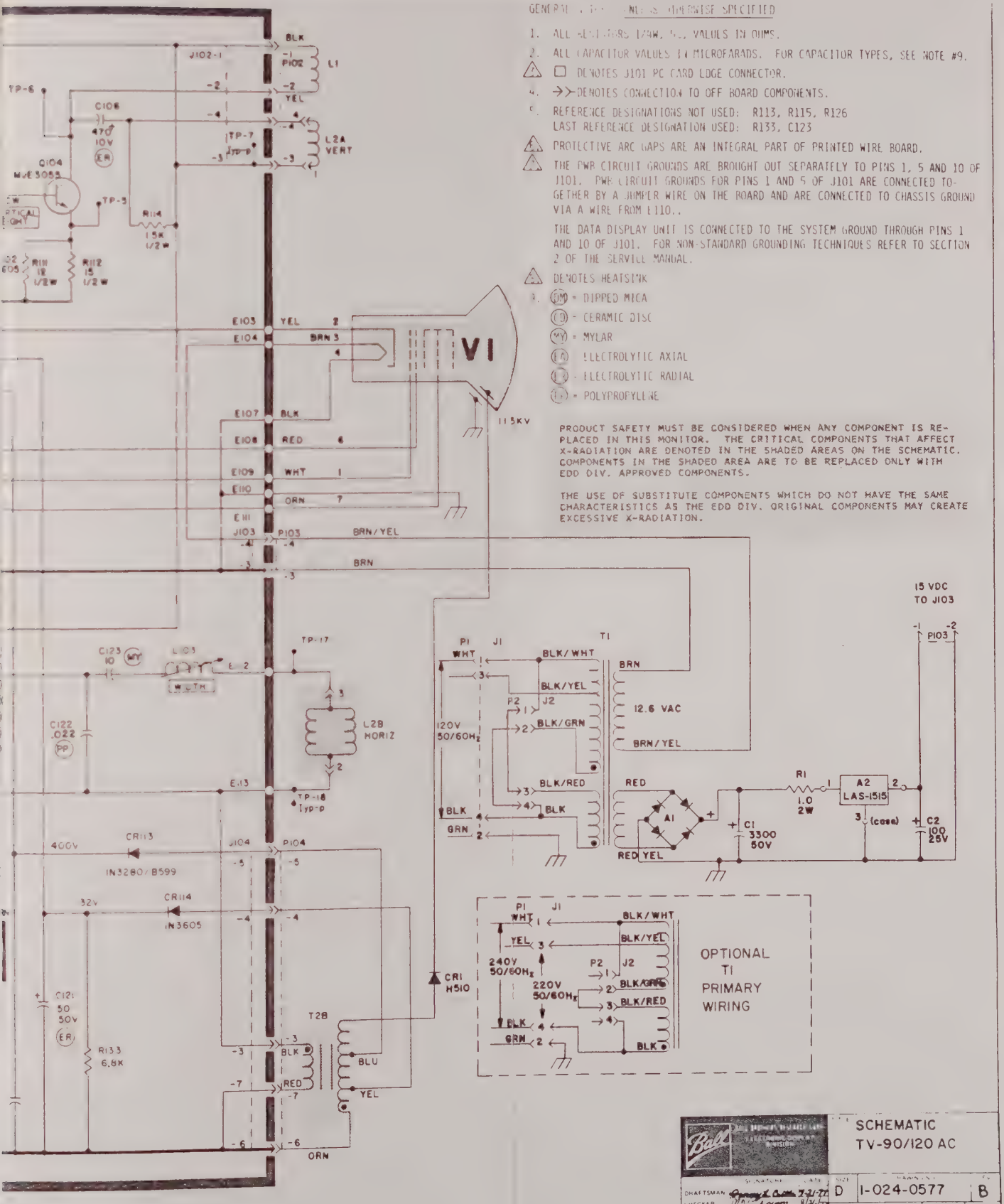


Figure TC 90/120


GENERAL NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS 1/4W, 5%, VALUES IN OHMS.
2. ALL CAPACITOR VALUES IN MICROFARADS. FOR CAPACITOR TYPES, SEE NOTE #9.
3. □ DENOTES J101 PC CARD EDGE CONNECTOR.
4. →→ DENOTES CONNECTION TO OFF BOARD COMPONENTS.
5. REFERENCE DESIGNATIONS NOT USED: R113, R115, R126
LAST REFERENCE DESIGNATION USED: R133, C123
6. PROTECTIVE ARC GAPS ARE AN INTEGRAL PART OF PRINTED WIRE BOARD.
7. THE PWB CIRCUIT GROUNDS ARE BROUGHT OUT SEPARATELY TO PINS 1, 5 AND 10 OF J101. PWB CIRCUIT GROUNDS FOR PINS 1 AND 5 OF J101 ARE CONNECTED TOGETHER BY A JUMPER WIRE ON THE BOARD AND ARE CONNECTED TO CHASSIS GROUND VIA A WIRE FROM E110..
THE DATA DISPLAY UNIT IS CONNECTED TO THE SYSTEM GROUND THROUGH PINS 1 AND 10 OF J101. FOR NON-STANDARD GROUNDING TECHNIQUES REFER TO SECTION 2 OF THE SERVICE MANUAL.
8. DENOTES HEATSINK
9. (DM) = DIPPED MICA
(CD) = CERAMIC DISC
(MY) = MYLAR
(EA) = ELECTROLYTIC AXIAL
(EL) = ELECTROLYTIC RADIAL
(PP) = POLYPROPYLENE
PRODUCT SAFETY MUST BE CONSIDERED WHEN ANY COMPONENT IS REPLACED IN THIS MONITOR. THE CRITICAL COMPONENTS THAT AFFECT X-RADIATION ARE DENOTED IN THE SHADED AREAS ON THE SCHEMATIC. COMPONENTS IN THE SHADED AREA ARE TO BE REPLACED ONLY WITH EDD DIV. APPROVED COMPONENTS.
THE USE OF SUBSTITUTE COMPONENTS WHICH DO NOT HAVE THE SAME CHARACTERISTICS AS THE EDD DIV. ORIGINAL COMPONENTS MAY CREATE EXCESSIVE X-RADIATION.
J102-1
P102
L1
TP-6
C108
470
10V
(ER)
Q104
MJE3055
TP-7
Typ-p
L2A
VERT
TP-5
R114
1.5K
1/2W
R111
1K
1/2W
R112
15
1/2W
E103
E104
E107
E108
E109
E110
E111
YEL
BRN
BLK
RED
WHT
ORN
V1
11.5KV
J103
P103
BRN/YEL
BRN
15 VDC
TO J103
C123
10
(MY)
L103
WIDTH
TP-17
L2B
HORIZ
C122
.022
(PP)
E113
TP-18
Typ-p
P1
J1
T1
WHT
BLK/WHT
BLK/YEL
BLK/GRN
BLK/RED
BLK
GRN
BRN
RED
YEL
120V
50/60Hz
12.6 VAC
BRN/YEL
P2
J2
R1
1.0
2W
A2
LAS-1515
(case)
A1
C1
3300
50V
C2
100
25V
400V
CR113
IN3280/B599
J104
P104
32V
CR114
IN3605
C121
50
50V
(ER)
R133
6.8K
T2B
BLK
BLU
RED
YEL
ORN
CR1
H510
OPTIONAL
TI
PRIMARY
WIRING
240V
50/60Hz
220V
50/60Hz
SCHEMATIC
TV-90/120 AC
D
1-024-0577
B
DRAFTSMAN
CHECKER
DESIGNER
ENGINEER
NONE
1 OF 2

PARTS LIST, TV 90/120 AC

REF SYM	DESCRIPTION	BBRC PART NUMBER	USED ON 6-002- 0696	0654	0714	0729
A1	INT CIRCUIT LAS-1515	1-025-0122	X	X	X	X
A2	BRIDGE RECTIFIER	1-021-0413	X	X	X	X
A101	RES TRIM, 60K, VERT HOLD	1-011-8006	X	X	X	X
A102	RES TRIM, 20K, VERT LIN	1-011-8005	X	X	X	X
A103	RES TRIM, 2.5K, VIDEO CENTER	1-011-8001	X	X	X	X
	CAPACITOR, FIXED, uF UNLESS NOTED					
C1	3300; 50V, E	1-012-2286	X	X	X	X
C2	100; 25V, E	1-012-2076	X	X	X	X
C101	100PF±5%, 500V, DM	1-012-0300	X	X	X	X
C102	.005±20%; 100V, CD	10-12-7508	X	X	X	X
C103	.22±10%; 100V, MY	1-012-2277	X	X	X	X
C104	.22±10%; 100V, MY	1-012-2277	X	X	X	X
C105	.68; 50V, E	1-012-2264	X	X	X	X
C106	470; 10V, E	1-012-2158	X	X	X	X
C107	NOT USED					
C108	25; 25V, E	1-012-1380	X	X	X	X
C109	.01±20%; 1000V, CD	1-012-2214	X	X	X	X
C110	.02±20%; 1000V, CD	1-012-2217	X	X	X	X
C111	.01±20%; 1000V, CD	1-012-2214	X	X	X	X
C112	.0022±10%; 630V, MY	1-012-2254	X	X	X	X
C113	.0047±10%; 630V, MY	1-012-2279	X	X	X	X
C114	.02±20%; 100V, CD	10-12-7209	X	X	X	X
C115	1; 50V, E	1-012-2189	X	X	X	X
C116	50; 50V, E	1-012-2157	X	X	X	X
C117	.047±10%; 250V, MY	1-012-2240	X	X	X	X
C118	220; 25V, E	1-012-2159	X	X	X	X
C119	10±10%; 100V, MY	1-012-2255	X	X	X	X
C120	.02±20%; 500V, CD	1-012-0780	X	X	X	X
C121	50; 50V, E	1-012-2157	X	X	X	X
C122	.022±10%; 250V, PP	1-012-2297	X	X	X	X
C123	10±10%; 100V, MY	1-012-2255	X	X	X	X
C124	NOT USED					
	DIODE					
CR	H510	1-021-0424	X	X	X	X
CR101	1N3605	1-021-0410	X	X	X	X
CR102	1N3605	1-021-0410	X	X	X	X
CR103	1N3605	1-021-0410	X	X	X	X
CR104	1N3605	1-021-0410	X	X	X	X
CR105	1N3605	1-021-0410	X	X	X	X
CR106	1N3605	1-021-0410	X	X	X	X
CR107	1N3605	1-021-0410	X	X	X	X
CR108	NOT USED					
CR109	1N3605	1-021-0410	X	X	X	X
CR110	1N3280/B599	1-021-0403	X	X	X	X
CR111	30S3	1-021-0458	X	X	X	X
CR112	30S3	1-021-0458	X	X	X	X
CR113	1N3280/B599	1-021-0403	X	X	X	X
CR114	1N3605	1-021-0410	X	X	X	X
	FUSE					
F101	NOT USED					
	CONNECTORS					
J102	CONNECTOR, 4 PIN MALE	1-039-0146	X	X	X	X
J103	CONNECTOR, 4 PIN MALE	1-039-0146	X	X	X	X
J104	CONNECTOR, 7 PIN MALE	1-039-0145	X	X	X	X

REF SYM	DESCRIPTION	PART NUMBER	USED ON 6-002- 0696	0654	0714	072
	COIL					
L1	VERTICAL CHOKE	6-003-0529	X	X	X	X
L2	DEFLECTION, TV 120/AC	1-023-0231		X	X	
	OR DEFLECTION, TV 90/AC	1-023-0237	X			X
L101	560uH	1-016-0302	X	X	X	X
L102	LINEARITY	1-016-0328	X	X	X	X
L103	WIDTH	1-016-0303	X	X	X	X
	TRANSISTOR					
Q101	2N5830	1-015-1172	X	X	X	X
Q102	2N6027	1-015-1157	X	X	X	X
Q103	MPS-A65	1-015-1186	X	X	X	X
Q104	MJE3055	1-015-1156	X	X	X	X
Q105	2N4124	1-015-1139	X	X	X	X
Q106	2N4124	1-015-1139	X	X	X	X
Q107	MPS-U05	1-015-1159	X	X	X	X
Q108	BU407	1-015-1210	X	X	X	X
	RESISTOR, FIXED, CARBON, ±5%; 1/4W UNLESS NOTED					
R101	47	70-16-0470	X	X	X	X
R102	100	70-16-0101	X	X	X	X
R103	47	70-16-0470	X	X	X	X
R104	220; 1/2W	1-011-2254	X	X	X	X
R105	820; 1/2W	1-011-2268	X	X	X	X
R106	470	70-16-0471	X	X	X	X
R107	360	70-16-0361	X	X	X	X
R108	100K	70-16-0104	X	X	X	X
R109	300; 1/2W	1-011-2257	X	X	X	X
R110	VAR; 250±20%; CO VERT HGT	70-89-0251	X	X	X	X
R111	12; 1/2W	1-011-2224	X	X	X	X
R112	15; 1/2W	1-011-2226	X	X	X	X
R113	NOT USED					
R114	1.5K; 1/2W	1-011-2274	X	X	X	X
R115	NOT USED					
R116	62K	70-16-0623	X	X	X	X
R117	VAR; 100K±20%; CO BRT ADJ	1-011-5435	X	X		
R118	30K; 1/2W	1-011-2305	X	X	X	X
R119	9.1K	70-16-0912	X	X	X	X
R120	8.2M	70-16-0825	X	X	X	X
R121	100K	70-16-0104	X	X	X	X
R122	VAR; 2.5M±20%, CO FOC ADJ	1-011-5566	X	X	X	X
R123	NOT USED					
R124	510	70-16-0511	X	X	X	X
R125	1K	70-16-0102	X	X	X	X
R126	NOT USED					
R127	3.3K	70-16-0332	X	X	X	X
R128	30K	70-16-0303	X	X	X	X
R129	3K	70-16-0302	X	X	X	X
R130	82±10; 3W, WW	1-011-2375	X	X	X	X
R131	3; 1/2W, CO	1-011-2478	X	X	X	X
R132	1.2±10%; 2W, WW	1-011-1395	X	X	X	X
R133	6.8K	70-16-0682	X	X	X	X
R134	NOT USED					
R135	NOT USED					
	TRANSFORMER					
T1	POWER	6-003-0569	X	X	X	X
T2	HIGH VOLTAGE	6-003-0530		X	X	
	OR HIGH VOLTAGE	6-003-0602	X			X
T101	HORIZ DRIVER	1-017-5402	X	X	X	X
VR101	ZENER, 1N759A, 12V	78-15-0759	X	X	X	X
	MISCELLANEOUS					
	CRT SOCKET	1-022-0427	X	X	X	X
	ASSY POWER SUPPLY	6-003-0570	X	X	X	X
	ASSY JUMPER PLUG	6-004-0749	X	X	X	X
	SOCKET TRANSISTOR	1-022-0433	X	X	X	X

Figure 6-8 TV 90/120 AC Parts List, Waveform and Component Layout

TP5
5V/DIV 2mS/DIV
1 1 VDC
TP4
2V DIV 2mS/DIV
3 VDC
TP2
10V DIV 10µS/DIV
31 4 VDC
TP6
20V/DIV 2mS/DIV
TP3
1V/DIV 2mS/DIV
3 72 VDC
TP7
TP1
.5V/DIV 10µS/DIV
.15VDC
TP18
2 V/DIV 10µS/DIV
14 7 VDC
TP8
1V/DIV 10µS/DIV
1.6 VDC
TP15
1V/DIV 10µS/DIV
13 8 VDC
TP9
5V/DIV 10µS/DIV
8 6 VDC
TP17
10V/DIV 10µS/DIV
1 VDC
TP10
2V/DIV 10µS/DIV
4 25 VDC
TP11
2V/DIV 10µS/DIV
34 VDC
TP14
50V/DIV 10µS/DIV
8 VDC
TP18
1A/DIV 10µS/DIV
TP12
5V/DIV 10µS/DIV
9 6 VDC
TP13
50V/DIV 10µS/DIV
8 VDC
0442D
J102
J104
J101
A101
A102
A103
T101
L101
L102
L103
C101
C102
C103
C104
C106
C108
C109
C110
C111
C112
C113
C114
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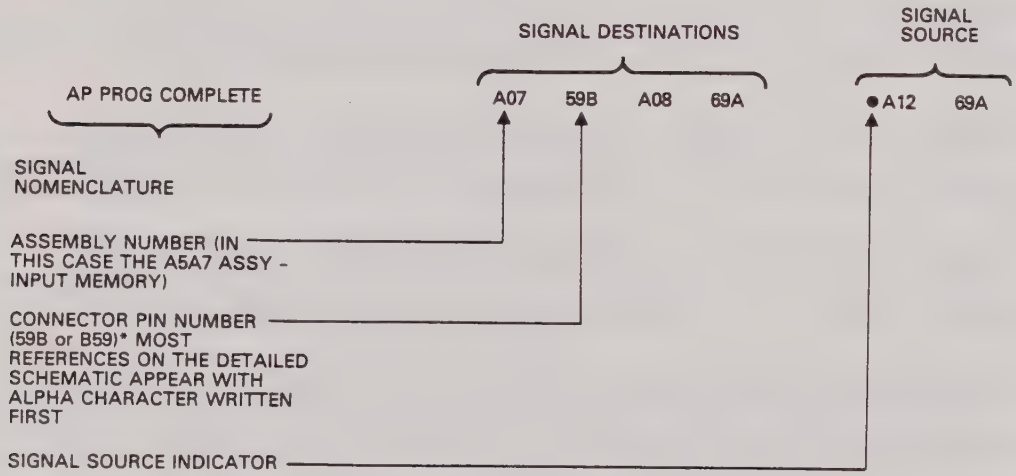
C117
C118
C119
C120
C121
C122
C123
R101
R102
R103
R104
R105
R106
R107
R108
R109
R110
R111
R112
R114
R116
R117
R118
R119
R120
R121
R122
R123
R124
R125
R127
R128
R130
R131
R132
Q101
Q102
Q103
Q106
Q107
Q108
VR101
CR101
CR102
CR103
CR104
CR105
CR106
CR107
CR108
CR109
CR110
CR111
CR112
CR113
CR114
E101
E102
E103
E104
E105
E106
E107
E108
E109
E110
E111
E112
E113
J10
OV

APPENDIX B

SD375 WIRE STRING LIST

The String List contained herein is an alphanumeric wiring interconnect table. It contains a comprehensive listing of all signal callouts which interface with more than one assembly within the SD375.

The String List has been provided to assist the service engineer or technician by indicating the source and destination of each interconnect and as an aid in using the detailed schematics of Volume II. The source of any signal is identified by the dot (•) which appears to the left of the assembly/pin reference designation as follows:


SIGNAL DESTINATIONS
SIGNAL SOURCE
AP PROG COMPLETE
A07 59B A08 69A
•A12 69A
SIGNAL NOMENCLATURE
ASSEMBLY NUMBER (IN THIS CASE THE A5A7 ASSY - INPUT MEMORY)
CONNECTOR PIN NUMBER (59B or B59)* MOST REFERENCES ON THE DETAILED SCHEMATIC APPEAR WITH ALPHA CHARACTER WRITTEN FIRST
SIGNAL SOURCE INDICATOR

SIGNAL NAME	STRING LIST CONNECTOR / PIN							
+12V	A19 01 ,	A19 02 ,	•PS1 25 ,	PS1 26 ,	PS1 27 ,	PS1 28		
+15V	A01 05B,	A01 06B,	A02 05B,	A02 06B,	A03 05B,	A03 06B,	A04 05B,	A04 06B,
	A05 05B,	A05 06B,	A06 05B,	A06 06B,	A07 05B,	A07 06B,	A08 05B,	A08 06B,
	A09 05B,	A09 06B,	A10 05B,	A10 06B,	A11 05B,	A11 06B,	A12 05B,	A12 06B,
	A13 05B,	A13 06B,	A14 05B,	A14 06B,	A15 05B,	A15 06B,	A16 05B,	A16 06B,
	A17 05B,	A17 06B,	A19 07 ,	A19 08 ,	PS1 43 ,	PS1 45 ,	PS1 47 ,	PS1 49 ,
	PS1 51 ,	•PS1 53 ,	PS1 55					
+5V	A01 05A,	A01 06A,	A01 67B,	A01 68B,	A02 05A,	A02 06A,	A02 67B,	A02 68B,
	A03 05A,	A03 06A,	A03 67B,	A03 68B,	A04 05A,	A04 06A,	A04 67B,	A04 68B,
	A05 05A,	A05 06A,	A05 67B,	A05 68B,	A06 05A,	A06 06A,	A06 67B,	A06 68B,
	A07 05A,	A07 06A,	A07 67B,	A07 68B,	A08 05A,	A08 06A,	A08 67B,	A08 68B,
	A09 05A,	A09 06A,	A09 67B,	A09 68B,	A10 05A,	A10 06A,	A10 67B,	A10 68B,
	A11 05A,	A11 06A,	A11 67B,	A11 68B,	A12 05A,	A12 06A,	A12 67B,	A12 68B,
	A13 05A,	A13 06A,	A13 67B,	A13 68B,	A14 05A,	A14 06A,	A14 67B,	A14 68B,
	A15 05A,	A15 06A,	A15 67B,	A15 68B,	A16 05A,	A16 06A,	A16 67B,	A16 68B,
	A17 05A,	A17 06A,	A17 67B,	A17 68B,	A18 05 ,	A18 06 ,	A18147 ,	A18148 ,
	A19 45 ,	A19 46 ,	•PS1 01 ,	PS1 02 ,	PS1 03 ,	PS1 04 ,	PS1 05 ,	PS1 06 ,
	PS1 07 ,	PS1 08 ,	PS1 09 ,	PS1 10 ,	PS1 11 ,	PS1 12		
+5V SENSE	A09 05A,	A09 06A,	PS1 24					
-15V	A01 95A,	A01 96A,	A02 95A,	A02 96A,	A03 95A,	A03 96A,	A04 95A,	A04 96A,
	A05 95A,	A05 96A,	A06 95A,	A06 96A,	A07 95A,	A07 96A,	A08 95A,	A08 96A,
	•A09 95A,	A09 96A,	A10 95A,	A10 96A,	A11 95A,	A11 96A,	A12 95A,	A12 96A,
	A13 95A,	A13 96A,	A14 95A,	A14 96A,	A15 95A,	A15 96A,	A16 95A,	A16 96A,
	A17 95A,	A17 96A,	A19 09 ,	A19 10 ,	PS1 44 ,	•PS1 46 ,	PS1 48 ,	PS1 50 ,
	PS1 52 ,	PS1 54 ,	PS1 56					
GND A	A01100A,	A01 99A,	A01 01B,	A01 02B,	A02100A,	A02 99A,	A02 01B,	A02 02B,
	A03100A,	A03 99A,	A03 01B,	A03 02B,	A04100A,	A04 99A,	A04 01B,	A04 02B,
	A05100A,	A05 99A,	A05 01B,	A05 02B,	A06100A,	A06 28A,	A06 30A,	A06 99A,
	A06 01B,	A06 02B,	A07100A,	A07 99A,	A07 01B,	A07 02B,	A08100A,	A08 99A,
	A08 01B,	A08 02B,	A09100A,	A09 99A,	A09 01B,	A09 02B,	A10100A,	A10 99A,
	A10 01B,	A10 02B,	A11100A,	A11 99A,	A11 01B,	A11 02B,	A12100A,	A12 99A,
	A12 01B,	A12 02B,	A13100A,	A13 99A,	A13 01B,	A13 02B,	A14100A,	A14 99A,
	A14 01B,	A14 02B,	A15100A,	A15 99A,	A15 01B,	A15 02B,	A16100A,	A16 99A,
	A16 01B,	A16 02B,	A16 34B,	A16 69B,	A17100A,	A17 99A,	A17 01B,	A17 02B,
	A19 05 ,	A19 06 ,	•PS1 33 ,	PS1 34 ,	PS1 35 ,	PS1 36 ,	PS1 39 ,	PS1 40 ,
	PS1 41 ,	PS1 42						
GND B	A01 01A,	A01 02A,	A01 80A,	A01 71B,	A01 72B,	A02 01A,	A02 02A,	A02 80A,
	A02 71B,	A02 72B,	A03 01A,	A03 02A,	A03 71B,	A03 72B,	A04 01A,	A04 02A,
	A04 71B,	A04 72B,	A05 01A,	A05 02A,	A05 71B,	A05 72B,	A06 01A,	A06 02A,
	A06 71B,	A06 72B,	A07 01A,	A07 02A,	A07 71B,	A07 72B,	A08 01A,	A08 02A,
	A08 71B,	A08 72B,	A09 01A,	A09 02A,	A09 71B,	A09 72B,	A10 01A,	A10 02A,
	A10 71B,	A10 72B,	A11 01A,	A11 02A,	A11 71B,	A11 72B,	A12 01A,	A12 02A,
	A12 71B,	A12 72B,	A13 01A,	A13 02A,	A13 71B,	A13 72B,	A14 01A,	A14 02A,
	A14 71B,	A14 72B,	A15 01A,	A15 02A,	A15 71B,	A15 72B,	A16 01A,	A16 02A,
	A16 71B,	A16 72B,	A17 01A,	A17 02A,	A17 71B,	A17 72B,	A18 01 ,	A18 02 ,
	A18151 ,	A18152 ,	A19 49 ,	A19 50 ,	A20 01 ,	A20 02 ,	A20 03 ,	A20 04 ,
	A20 25 ,	A20 27 ,	A20 31 ,	A20 33 ,	A20 35 ,	A20 39 ,	A20 41 ,	A20 45 ,
	A20 47 ,	E01 ,	E03 ,	E05 ,	E07 ,	E09 ,	E11 ,	E13 ,
	E16 ,	E18 ,	E20 ,	J19 17 ,	J19 33 ,	J19 35 ,	J19 37 ,	J19 39 ,

I----SIGNAL NAME----I		I----------STRING LIST CONNECTOR / PIN----------I							
		J19 41 ,	J19 43 ,	J19 45 ,	J19 47 ,	J19 49 ,	J20 18 ,	J20 19 ,	J20 20 ,
		J20 21 ,	J20 22 ,	J20 23 ,	J20 24 ,	J21 01 ,	J22 61 ,	J22 62 ,	J23 63 ,
		•PS1 13 ,	PS1 14 ,	PS1 15 ,	PS1 16 ,	PS1 17 ,	PS1 18 ,	PS1 19 ,	PS1 20 ,
		PS1 21 ,	PS1 22						
+1		A18 09 ,	•J22 04						
A/D A SIGN		•A01 70A,	A02 58A,	A03 58A,	A04 58A,	A05 58A,	A06 58A,	A07 58A	
A/D A 2**-01		•A01 69A,	A02 57A,	A03 57A,	A04 57A,	A05 57A,	A06 57A,	A07 57A	
A/D A 2**-02		•A01 68A,	A02 56A,	A03 56A,	A04 56A,	A05 56A,	A06 56A,	A07 56A	
A/D A 2**-03		•A01 67A,	A02 55A,	A03 55A,	A04 55A,	A05 55A,	A06 55A,	A07 55A	
A/D A 2**-04		•A01 66A,	A02 54A,	A03 54A,	A04 54A,	A05 54A,	A06 54A,	A07 54A	
A/D A 2**-05		•A01 65A,	A02 53A,	A03 53A,	A04 53A,	A05 53A,	A06 53A,	A07 53A	
A/D A 2**-06		•A01 64A,	A02 52A,	A03 52A,	A04 52A,	A05 52A,	A06 52A,	A07 52A	
A/D A 2**-07		•A01 63A,	A02 51A,	A03 51A,	A04 51A,	A05 51A,	A06 51A,	A07 51A	
A/D A 2**-08		•A01 62A,	A02 50A,	A03 50A,	A04 50A,	A05 50A,	A06 50A,	A07 50A	
A/D A 2**-09		•A01 61A,	A02 49A,	A03 49A,	A04 49A,	A05 49A,	A06 49A,	A07 49A	
A/D A 2**-10		•A01 60A,	A02 48A,	A03 48A,	A04 48A,	A05 48A,	A06 48A,	A07 48A	
A/D A 2**-11		•A01 59A,	A02 47A,	A03 47A,	A04 47A,	A05 47A,	A06 47A,	A07 47A	
A/D B SIGN		•A02 70A,	A03 70A,	A04 70A,	A05 70A,	A06 70A,	A07 70A		
A/D B 2**-01		•A02 69A,	A03 69A,	A04 69A,	A05 69A,	A06 69A,	A07 69A		
A/D B 2**-02		•A02 68A,	A03 68A,	A04 68A,	A05 68A,	A06 68A,	A07 68A		
A/D B 2**-03		•A02 67A,	A03 67A,	A04 67A,	A05 67A,	A06 67A,	A07 67A		
A/D B 2**-04		•A02 66A,	A03 66A,	A04 66A,	A05 66A,	A06 66A,	A07 66A		
A/D B 2**-05		•A02 65A,	A03 65A,	A04 65A,	A05 65A,	A06 65A,	A07 65A		
A/D B 2**-06		•A02 64A,	A03 64A,	A04 64A,	A05 64A,	A06 64A,	A07 64A		
A/D B 2**-07		•A02 63A,	A03 63A,	A04 63A,	A05 63A,	A06 63A,	A07 63A		
A/D B 2**-08		•A02 62A,	A03 62A,	A04 62A,	A05 62A,	A06 62A,	A07 62A		
A/D B 2**-09		•A02 61A,	A03 61A,	A04 61A,	A05 61A,	A06 61A,	A07 61A		
A/D B 2**-10		•A02 60A,	A03 60A,	A04 60A,	A05 60A,	A06 60A,	A07 60A		
A/D B 2**-11		•A02 59A,	A03 59A,	A04 59A,	A05 59A,	A06 59A,	A07 59A		
A/D OVERLOAD A	*P	•A01 30A,	A08 60A						
A/D OVERLOAD B	*P	•A02 30A,	A08 59A						
AC	*	A01 69B,	A02 69B,	A03 69B,	•A18138				
ADDRESS OFFSET 2**0		A04 29A,	•A05 29A						
ADDRESS OFFSET 2**1		A04 30A,	•A05 30A						
ADDRESS OFFSET 2**2		A04 31A,	•A05 31A						
ADDRESS OFFSET 2**3		A04 32A,	•A05 32A						
ADDRESS OFFSET 2**4		A04 33A,	•A05 33A						
ADDRESS OFFSET 2**5		A04 34A,	•A05 34A						
ADDRESS OFFSET 2**6		A04 35A,	•A05 35A						
ADDRESS OFFSET 2**7		A04 36A,	•A05 36A						
ADDRESS OFFSET 2**8		A04 37A,	•A05 37A						
ADDRESS OFFSET 2**9		A04 38A,	•A05 38A						
ALT MEMORY		A11 25A,	•A13 28A						
AP HALT ACK	*P	A08 63A,	•A12 50A						
AP HALT REQUEST		•A08 21A,	A11 22A						
AP PROG COMPLETE	*P	A07 59B,	A08 69A,	•A12 69A					
AP READ 1024 PULSE	*P	A07 58B,	A08 68A,	•A12 68A					
AR OFFSET		A01 26B,	A02 26B,	A03 26B,	A04 26B,	A05 26B,	•A06 26B		
AR 10**2		A01 33B,	A02 33B,	A03 33B,	A04 33B,	A05 33B,	•A06 33B		

SIGNAL NAME		STRING LIST CONNECTOR / PIN
AR 100 KHZ		A01 34B, A02 34B, A03 34B, A04 34B, A05 34B, •A06 34B
AR 100KHZ TO A1		•A06 60B
AR 2**0		A01 27B, A02 27B, A03 27B, A04 27B, A05 27B, •A06 27B
AR 2**1		A01 28B, A02 28B, A03 28B, A04 28B, A05 28B, •A06 28B
AR 2**2		A01 29B, A02 29B, A03 29B, A04 29B, A05 29B, •A06 29B
AR 2**3		A01 30B, A02 30B, A03 30B, A04 30B, A05 30B, •A06 30B
AR 2**4		A01 31B, A02 31B, A03 31B, A04 31B, A05 31B, •A06 31B
AR 2**5		A01 32B, A02 32B, A03 32B, A04 32B, A05 32B, •A06 32B
ATN		•A09 19A, E04 , J19 34 , J20 11
B READ I/O	P	•A08 03A, A09 66A
BATTERY VOLTAGE		A08 45A, •PS1 38
BEEPER	*	•A08 18A, A18146
BUFF READ 2**0		A04 69B, •A05 69B
BUFF READ 2**1		A04 70B, •A05 70B
CAC CLOCK	*P	•A12 19A, A15 19A
CAL MODE		•A08 20A, A14 16A
CAL SIG		A01 66B, A02 66B, •A06 27A, A06 29A
CHARACTER MEM CS	*P	•A08 29B, A16 24B
CHARACTER OFF	*	A16 04A, •A20 52
CKWC	*P	A04 46A, •A05 46A
CLK ADDR SEL REG	*P	•A12 27A, A15 27A
CLK PULSE CODE	*P	•A11 89A, A12 90A
CLK SOURCE	*P	•A06 11B, A07 11B
CLK SW LATCH	*P	•A11 58B, A18101
CLR ADDR COUNTER	*P	•A14 88A, A16 88A
CLR EN MULTIPLY COMPLETE	*P	A10 36A, •A12 35A
CLR SHIFT CONTROL	*P	A10 26A, •A12 26A
COMPOSITE VIDEO		•A16 70B, A19 11 , A20 50
CONTRAST		A16 20B, •A19 38
CONVERT COMPLETE A	*P	•A01 87A, A06 87A, A07 87A
CONVERT COMPLETE B	*P	•A02 87A, A06 88A, A07 88A
CONVERT COMPLETE XLATOR	*P	A04 04A, •A06 04A
CPE ADDR EN	*	•A12 67A, A15 67A
CPE DATA EN	*	•A11 69A, A12 70A
CPE OVERFLOW SLICE 5		A11 37A, •A12 38A
CPE OVERFLOW SLICE 6		A11 39A, •A12 40A
CPE UNDERFLOW SLICE 6		A11 35A, •A12 36A
CTR SEL 2**0		A04 11B, •A05 11B
CTR SEL 2**1		A04 12B, •A05 12B
CTS		A09 28A, •J21 05
CURSOR CLK 2**0		•A14 19B, A16 32B
CURSOR LEFT	*P	•A08 38A, A14 38A
CURSOR MODE 2**0		A15 63B, •A18 37
CURSOR MODE 2**1		A15 64B, •A18 36
CURSOR MODE 2**2		A15 65B, •A18 35
CURSOR MOTION	*	A14 62B, •A18 38
CURSOR ON SWEEP		A13 21B, •A14 22B
CURSOR RIGHT	*P	•A08 37A, A14 37A
DATA		•A11 43A

SIGNAL NAME		STRING LIST CONNECTOR / PIN
DATA I/O -1		•A09 03A, J19 01 , J20 01
DATA I/O -10		•A09 23A, J19 10
DATA I/O -11		•A09 24A, J19 11
DATA I/O -12		•A09 32A, J19 12
DATA I/O -13		•A09 33A, J19 13
DATA I/O -14		•A09 35A, J19 14
DATA I/O -15		•A09 36A, J19 15
DATA I/O -16		•A09 38A, J19 16
DATA I/O -2		•A09 04A, J19 02 , J20 02
DATA I/O -3		•A09 07A, J19 03 , J20 03
DATA I/O -4		•A09 08A, J19 04 , J20 04
DATA I/O -5		•A09 09A, J19 05 , J20 13
DATA I/O -6		•A09 10A, J19 06 , J20 14
DATA I/O -7		•A09 11A, J19 07 , J20 15
DATA I/O -8		•A09 12A, J19 08 , J20 16
DATA I/O -9		•A09 21A, J19 09
DATA MEM EN	*	•A11 09A, A13 09A, A15 09A
DATA TO XLATOR SIGN		A04 22A, •A06 22A
DATA TO XLATOR 2**-01		A04 21A, •A06 21A
DATA TO XLATOR 2**-02		A04 20A, •A06 20A
DATA TO XLATOR 2**-03		A04 19A, •A06 19A
DATA TO XLATOR 2**-04		A04 18A, •A06 18A
DATA TO XLATOR 2**-05		A04 17A, •A06 17A
DATA TO XLATOR 2**-06		A04 16A, •A06 16A
DATA TO XLATOR 2**-07		A04 15A, •A06 15A
DATA TO XLATOR 2**-08		A04 14A, •A06 14A
DATA TO XLATOR 2**-09		A04 12A, •A06 12A
DATA TO XLATOR 2**-10		A04 10A, •A06 10A
DATA TO XLATOR 2**-11		A04 08A, •A06 08A
DAV		•A09 14A, E14 , J19 44 , J20 06
DELTA X MODE		A14 25A, •A15 26A
DELTA X SET		•A08 09A, A13 27A
DISABLE MULTIPLY SHIFT		A10 37A, •A11 36A
DISPLAY MODE 2**0		A14 64B, •A18 42
DISPLAY MODE 2**1		A14 65B, •A18 40
DISPLAY MODE 2**2		A14 66B, •A18 39
DISPLAY REQUEST CLK		•A06 92A, A14 98A
DMA READY INPUT		A08 09B, •A09 10B
DSR		A09 29A, •J21 06
DTR		•A09 34A, J21 20
EDIT MODE		A14 27A, •A15 28A
EN CH A TO XLATOR	*	•A04 23A, A06 23A
EN CO - QUAD	*	A13 29B, •A14 32B
EN CURSOR	*P	•A08 24B, A14 34B
EN KEYBOARD 1	*	•A08 27B, A18133
EN KEYBOARD 2	*	•A08 26B, A18134
EN PLOTTER X	*P	•A03 16B, A08 23B, A13 32B
EN PLOTTER Y	*P	•A03 17B, A08 22B, A13 31B
EN SW CODE	*	•A11 24A, A18 60

I----SIGNAL NAME----I		I----------STRING LIST CONNECTOR / PIN----------I
EN XLATOR DATA	*	A04 17B, A05 17B, •A08 25B
EN 3000 MAILBOX		•A08 28B, A18102
ENABLE E	*	•A11 17A
ENABLE F	*	•A11 15A
ENABLE LINE CURSOR		A13 61B, •A14 61B
ENABLE RELATIVE ZERO	*P	•A06 10B, A07 10B
END CURRENT STAGE	*P	A10 18A, •A12 17A, A15 17A
ENSEMBLE # SEL		A11 48A, •A12 48A
ENSEMBLE CNT 0	*P	A08 54A, •A11 50A
EOI		•A09 13A, J19 46 , J20 05
ERASE	*	A18 08 , •J22 01
EXCITATION		•A20 05 , J19 64
EXECUTE	*P	•A07 98A, A10 98A, A11 98A, A13 98A, A15 94A, A17 98A
EXPAND SWEEP		•A13 25A, A14 26A
EXPO BUS EN	*	•A11 14A, A13 14A
EXT INTERRUPT		A11 11A, •A17 11A
EXT RESET	*	•A08 04A
EXT SAMPLE FREQ		A06 13A, •J22 09
EXT TIME DOMAIN SYNC	*P	•A20 42
EXT TIME DOMAIN SYNC¤+¤	*P	•A06 09A
EXT TIME DOMAIN SYNC¤-¤		•A06 32A
EXT TRANS CAPT ARM	*	A18 11 , •J22 06
EXT TRANS CAPT SEL	*	A06 07A, •J22 12
EXT TRANS CAPT TRIG	P	A06 03A, •J22 13
FILTERED SIG 100K -1		A01 27A, •A03 27A
FILTERED SIG 100K -2		A02 27A, •A03 28A
FPU DELTA EXPO EN	*	A10 29A, •A11 30A
FPU SHIFTER EN	*	A10 27A, •A11 28A
FREEZE		•A08 19A, A11 07A, A14 07A, A15 07A
FREEZE HARMONICS		A13 19B, •A14 20B
FUND CUR EN	*	•A11 12A, A14 12A
GND SENSE		•A11 01A, A11 02A, PS1 23
GRID		A16 07B, •A19 37
HARMONIC	*	A14 19A, •A15 20A
HARMONIC MODE		A14 21A, •A15 22A
HORIZ BLANK		•A16 08A, J22 49
HORIZ CRT DATA 2**0		•A13 51B
HORIZ CRT DATA 2**1		•A13 52B
HORIZ CRT DATA 2**2		•A13 53B
HORIZ CRT DATA 2**3		•A13 54B
HORIZ CRT DATA 2**4		•A13 55B
HORIZ CRT DATA 2**5		•A13 56B
HORIZ CRT DATA 2**6		•A13 57B
HORIZ CRT DATA 2**7		•A13 58B
HORIZ CRT DATA 2**8		•A13 59B
HORIZ CRT DATA 2**9		•A13 60B
HORIZONTAL DRIVE		•A16 31B, A19 21 , J22 48
I BUS 00		•A11 28B, A12 28B, A13 28B, A14 28B, A15 28B, A16 28B, A17 28B
I BUS 01		•A11 27B, A12 27B, A13 27B, A14 27B, A15 27B, A16 27B, A17 27B

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I BUS 02		•A11 26B, A12 26B, A13 26B, A14 26B, A15 26B, A16 26B, A17 26B
I BUS 03		•A11 25B, A12 25B, A13 25B, A14 25B, A15 25B, A16 25B, A17 25B
I BUS 04		•A11 24B, A12 24B
I BUS 05		•A11 23B, A12 23B
I BUS 06		•A11 22B, A12 22B
I BUS 07		•A11 21B, A12 21B
I BUS 08		•A11 20B, A12 20B
I BUS 09		•A11 19B, A12 19B
I BUS 10		•A11 18B, A12 18B
I BUS 11		•A11 17B, A12 17B
I BUS 12		•A11 16B, A12 16B
I BUS 13		•A11 15B, A12 15B
I BUS 14		•A11 14B, A12 14B
I BUS 15		•A11 13B, A12 13B
I BUS 16		•A11 12B, A12 12B
I BUS 17		•A11 11B, A12 11B
I BUS 18		•A11 10B, A12 10B
I BUS 19		•A11 09B, A12 09B
I BUS 20		•A11 08B, A12 08B
I/O ADDR SEL	*	A09 93A, •A13 94A
I/O ADDR SEL B		A09 91A, •A13 92A
I/O CARD	*	A08 49A, •A09 60A
I/O INTERRUPT ACK	*	•A08 17B, A09 18B
I/O INTERRUPT EN INPUT	*	•A08 11B, A09 11B
I/O INTERRUPT 1	*	A08 12B, •A09 12B
I/O MEM EN	*	A09 42A, •A11 42A
I/O PROM EN 1	*P	•A08 34 , A09 34
I/O PROM EN 2	*P	•A08 33 , A09 33
I/O RAM EN 1	*P	•A08 32 , A09 32
I/O RAM EN 2	*P	•A08 31 , A09 31B
I/O RAM 3		•A08 58A, A09 58A
I/O RAM 4	*P	•A08 46A, A09 46A
IFC		A09 17A, E08 , J19 38 , •J20 09
INITIALIZE		•A12 39A, A15 34A
INPUT ACK		•A07 97A, A11 97A
INPUT DATA EN A	*	A07 91A, •A11 92A
INPUT DATA EN B	*	A07 93A, •A11 94A
INPUT DATA RDY		•A04 41A, A05 42A
INPUT LEVEL A 2**0		A01 22B, A02 18B, A03 18B, A04 18B, A05 18B, •A06 18B
INPUT LEVEL A 2**1		A01 23B, A02 19B, A03 19B, A04 19B, A05 19B, •A06 19B
INPUT LEVEL A 2**2		A01 24B, A02 20B, A03 20B, A04 20B, A05 20B, •A06 20B
INPUT LEVEL A 2**3		A01 25B, A02 21B, A03 21B, A04 21B, A05 21B, •A06 21B
INPUT LEVEL B 2**0		A02 22B, A03 22B, A04 22B, A05 22B, •A06 22B
INPUT LEVEL B 2**1		A02 23B, A03 23B, A04 23B, A05 23B, •A06 23B
INPUT LEVEL B 2**2		A02 24B, A03 24B, A04 24B, A05 24B, •A06 24B
INPUT LEVEL B 2**3		A02 25B, A03 25B, A04 25B, A05 25B, •A06 25B
INPUT PROC FILE ADDR 20		•A05 03A, A07 03A
INPUT PROC FILE ADDR 21		•A05 04A, A07 04A
INPUT PROCESSOR CLK		•A06 59B, A07 61B

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INPUT REQUEST	*P	A07 92A, •A12 89A
INPUT SECTION ADDR EN	*P	A06 17B, •A08 30B
INT 1	*P	•A08 50A
INT 2	*P	•A08 51A
INT 3	*P	•A08 52A
INT 4	*P	•A08 53A
INT 5	*P	•A08 61A
INT 6	*P	•A08 62A
INTENSIFY DOT	*	A13 17A, •A14 18A
INTENSIFY LINE	*	A13 19A, •A14 20A
LD ADDR SEL COUNTER	*P	•A12 21A, A15 21A
LD DAC REG		A03 70B, •A14 29B
LD DATA READY	*P	•A12 13A, A14 13A
LD ENSEMBLE COUNTER	*P	•A08 21B, A12 30B
LD EXPO REG	*P	•A12 37A, A13 38A
LD FPU # SHIFTS	*P	A10 30A, •A12 30A
LD FPU DATA	*P	A10 28A, •A12 28A
LD MULTIPLY #1	*P	A10 20A, •A12 18A
LD MULTIPLY #2	*P	A10 22A, •A12 22A
LD SINE ADDR REG	*P	A12 25A, •A15 25A
LD STATUS	*P	•A04 16B, A05 16B
LD WRITE CNTR A	*	•A06 64B, A07 64B
LD WRITE CNTR B	*	•A06 65B, A07 65B
LD X GRID 1	*P	•A08 19B, A16 22B
LD X GRID 2	*P	•A08 18B, A16 21B
LD Y GRID	*P	•A08 20B, A16 23B
LDDC	*P	A04 94A, •A05 93A
LDNR	*P	A04 91A, •A05 92A
LDR1	*	A04 87A, •A05 88A
LDR2	*	A04 93A, •A05 94A
LDUC	*P	A04 97A, •A05 98A
LED EN 1	*P	•A08 08B, A18131
LED EN 2	*P	•A08 69B, A18132
LOAD XLATOR DATA	*P	•A05 15B, A07 20B
MASTER RESET	*P	A04 25A, A05 25A, A06 25A, A07 22A, •A08 22A, A09 22A, A10 44A, A11 44A, A12 44A, A13 29A, A14 29A, A15 29A, A16 29A, A17 29A
MATCH 1	*	A06 40A, •A17 32B
MATCH 2	*	A06 41A, •A17 33B
MEM A HOLD		•A06 62B, A07 62B
MEM B HOLD		•A06 63B, A07 63B
MEM HOLD A	*	A18 12 , •J22 05
MEM HOLD B	*	A18 14 , •J22 08
MEMORY ADDRESS A10		A04 98A, •A05 97A
MEMORY ADDRESS A11		A04 45A, •A05 45A
MODE CLK	*P	•A08 70A, A18108
MULT CLK		A05 07B, •A06 35A, A10 34A
MULTIPLY BYPASS EN	*	A10 25A, •A11 26A
MULTIPLY 2**-14		•A10 91A, A12 92A
MIC	*P	•A08 57A, A09 57A

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NDAC		•A09 16A, E10 , J19 40 , J20 08
NEW ENSEMBLE READY 1/1		•A07 31A, A11 31A
NEW ENSEMBLE READY 1/2		•A07 32A, A11 32A
NEW ENSEMBLE READY 1/4		•A07 30A, A11 16A
NEW ENSEMBLE READY 3/4		•A07 29A, A11 23A
NORM CURSOR EN	*	•A11 10A, A14 10A
NORMALIZED SIG 1		•A01 85A, A03 88A
NORMALIZED SIG 2		•A02 85A, A03 87A
NOT HARMONICS		•A12 15A, A13 18A
NRFD		•A09 15A, E12 , J19 42 , J20 07
OL2		•A08 10A
OP1	*P	•A08 34A
OP2	*P	•A08 33A
OP3	*P	•A08 32A
OP4	*P	•A08 31A
OP6	*P	•A08 35A
OUT 1		•A09 39A, J21 11
OUT 2		•A09 40A, J21 18
OUTPUT OVLD	*P	A08 93A, •A12 42A
OVERFLOW EN	*P	A10 17A, •A11 18A
OVERFLOW TEST	*P	A10 23A, •A12 24A
PEN LIFT-1		•A03 15A, A20 14
PEN LIFT-2		•A03 13A, A20 12
PFI	*	A08 47A, •PS1 37
PHASE 1 CLK		•A06 69B, A07 69B, A09 69B, A10 69B, A11 69B, A12 69B, A13 69B, A14 69B, A15 69B, A17 69B
PHASE 2 CLK		•A06 70B, A07 70B, A09 70B, A11 70B, A12 70B, A13 70B, A14 70B, A15 70B, A17 70B
PLOTTER DATA READY	*P	A08 64A, A13 33B, •A14 33B
PLOTTER X		•A03 21A, A20 18
PLOTTER Y		•A03 17A, A20 16
PLOTTING		•A08 15A, A11 41A, A14 15A
POWER ON RESET	P	•A03 22A, A08 28A
PRODUCT EN	*	A10 19A, •A11 20A, A12 20A
PROGRAM RESET	*P	• •A12 31A
PULSE ALTERNATE MEM	*P	•A12 43A, A13 36A
RAMDIS	P	•A08 10B, A18106
RANGE GT 5 KHZ		•A06 07B, A07 08B
RECEIVED DATA		A09 26A, •J21 03
REFRESH WRITE CPU	*	A13 23A, •A14 24A
REFRESH WRITE CRT	*	A13 21A, •A14 22A
REMOTE SHUTDOWN		•A12 56B, PS1 29
REN		A09 20A, J19 48 , •J20 17
RESET TRANS CAPT	P	A06 34A, •A07 33A
RETRACE BLANK		•A14 30B
RING INDICATOR		A09 30A, •J21 22
RIOWR	P	•A08 70B, A18100
RLSD		A09 31A, •J21 08
ROM SIM CLK SEL	*	A06 39A, •A17 31B

SIGNAL NAME		STRING LIST CONNECTOR / PIN
ROM SIM CONNECT	*	A06 37A, •A17 29B
RTS		•A09 27A, J21 04
SAMPLE FREQUENCY		A01 94A, A02 94A, A03 94A, •A06 94A, J19 26
SAMPLING FREQUENCY CHB		•A06 90A
SD420 VIDEO		•A16 10A, J22 47
SEL COUNTER ADDR SOURCE		A13 70A, •A14 70A
SEL EXT SAMPLE FREQUENCY	*	A06 11A, •A08 88A, •J22 10
SEL SD 346	*	A08 87A, •J22 22
SELECT REFRESH A	*	•A13 23B, A14 23B
SELECT REFRESH B	*	•A13 22B, A14 24B
SELECT RELATIVE ZERO A OR B	*	•A06 09B, A07 09B
SELECT 0	*P	•A11 70A, A17 70A
SELECT 1	*P	•A11 91A, A12 91A
SELECT 5	*P	•A11 87A, A12 88A
SET MEM A TO HOLD	*P	A06 14B, •A07 14B
SET MEM B TO HOLD	*P	A06 13B, •A07 13B
SHIELD		E02 , •J20 12
SHIFT BIT SET		A11 33A, •A12 34A
SHIFT DONE		•A10 41A, A11 13A
SIGN TEST		A11 34A, •A12 33A
SIGNAL IN A		•AC1 60B
SIGNAL IN B		•A02 60B
SINE DITHER		A01 08B, A02 08B, A03 08B, •A06 08B
SINGLE LINE TEST		•A08 16A, A11 59B
SINGLE STEP	*	A06 38A, •A17 30B
SINGLE STEP EN	*	A06 42A, •A17 34B
SPARE A14-A15		•A14 23A, A15 24A
SPARE A18-A8 #1		•A08 07B, A18112
SPARE A6-A7	*	•A06 12B, A07 12B
SRQ		•A09 18A, E06 , J19 36 , J20 10
START/AVERAGE	*	A18 07 , •J22 02
STAT 2	*P	•A08 92A
STAT 3	*P	•A08 91A
STAT 4	*P	•A08 90A
STAT 5	*	•A08 89A
STEP ADDR COUNTER	P	•A14 89A, A16 89A
STOP	*	A18 04 , •J22 18
SW CODE A0		A11 60B, •A18 71
SW CODE A1		A11 61B, •A18 72
SW CODE A2		A11 62B, •A18 69
SW CODE A3		A11 63B, •A18 70
SW CODE A4		A11 64B, •A18 67
SW CODE A5		A11 65B, •A18 68
SW CODE A6		A11 66B, •A18 65
SW CODE A7		A11 57B, •A18 66
SW SELECT MSB		A12 66B, •A18 44
SW SELECT 2**0		A08 11A, •A12 60B, A18 51
SW SELECT 2**1		A08 12A, •A12 61B, A18 52
SW SELECT 2**2		A08 13A, •A12 62B, A18 49

I----SIGNAL NAME----I		I----------STRING LIST CONNECTOR / PIN----------I
SW SELECT 2**3		•A08 14A, A12 63B, A18 50
SW SELECT 2**4		•A12 64B, A18 47
SW SELECT 2**5		•A12 65B, A18 48
SW SELECT 2**6		•A12 57B, A18 45
SW SELECT 2**7		•A12 58B, A18 46
TEST	*	A01 64B, A02 64B, •A18137
TEST 01		•A14 30A
TEST 18		•A11 21A
TEST 21		•A11 27A
TIME	*	A06 91A, •A14 94A
TRANS CAPT AT 90%		•A06 33A, A07 34A
TRANS CAPT AUTO	*	A18 10 , •J22 03
TRANS CAPT END	*P	•A06 45A, A08 65A
TRANS CAPT START	*P	•A06 46A, A08 66A
TRANS CAPT TRIG		•A06 58B, A07 60B
TRANSMITTED DATA		•A09 25A, J21 02
TV GND		A19 03 , A19 04 , •PS1 30 , PS1 31 , PS1 32
TV MEM ADDR MSB		•A14 92A, A16 92A
TV MEM CS 1	*	•A14 90A, A16 90A
TV MEM CS 2	*	•A14 91A, A16 91A
TV MEM CURSOR		•A13 17B, A14 17B, A15 17B, A16 17B
TV MEM DATA 2**0		•A13 08B, A14 08B, A15 08B, A16 08B
TV MEM DATA 2**1		•A13 09B, A14 09B, A15 09B, A16 09B
TV MEM DATA 2**2		•A13 10B, A14 10B, A15 10B, A16 10B
TV MEM DATA 2**3		•A13 11B, A14 11B, A15 11B, A16 11B
TV MEM DATA 2**4		•A13 12B, A14 12B, A15 12B, A16 12B
TV MEM DATA 2**5		•A13 13B, A14 13B, A15 13B, A16 13B
TV MEM DATA 2**6		•A13 14B, A14 14B, A15 14B, A16 14B
TV MEM DATA 2**7		•A13 15B, A14 15B, A15 15B, A16 15B
TV MEM DATA 2**8		•A13 16B, A14 16B, A15 16B, A16 16B
TV MEM LINE		•A13 18B, A14 18B, A15 18B, A16 18B
TV MEM WRITE	*P	•A14 87A, A16 87A
TV VERTICAL RETRACE	*P	A08 67A, A14 69A, •A16 69A, A19 22 , J22 46
UPPER GAIN #1		A03 14B, •A19 30
UPPER GAIN #2		A03 12B, •A19 26
UPPER OFFSET		A03 10B, •A19 25
UPPER TRACE		A03 66B, A13 63B, A14 63B, •A18 41
VERT BLANK		•A16 29B
VERTICAL DATA LSB		•A13 07B
VIDEO		•A16 33B, A19 12
WR	*P	A08 17A, •A18105
WRITE ADDR RAM	*P	•A12 23A, A15 23A
WRITE TRANS MEM		A04 43A, •A05 44A
X-ADDR 00		A13 39A, •A14 39A
X-ADDR 01		A13 40A, •A14 40A
X-ADDR 02		A13 41A, •A14 41A
X-ADDR 03		A13 42A, •A14 42A
X-ADDR 04		A13 43A, •A14 43A
X-ADDR 05		A13 44A, •A14 44A

SIGNAL NAME		STRING LIST CONNECTOR / PIN
X-ADDR 06		A13 45A, •A14 45A
X-ADDR 07		A13 46A, •A14 46A
X-ADDR 08		A13 47A, •A14 47A
X-ADDR 09		A13 48A, •A14 48A
X-ADDR 10		A13 50A, •A14 50A
XLATED DATA SIGN		•A05 20A, A07 20A
XLATED DATA 2**-01		•A05 19A, A07 19A
XLATED DATA 2**-02		•A05 18A, A07 18A
XLATED DATA 2**-03		•A05 17A, A07 17A
XLATED DATA 2**-04		•A05 16A, A07 16A
XLATED DATA 2**-05		•A05 15A, A07 15A
XLATED DATA 2**-06		•A05 14A, A07 14A
XLATED DATA 2**-07		•A05 13A, A07 13A
XLATED DATA 2**-08		•A05 12A, A07 12A
XLATED DATA 2**-09		•A05 11A, A07 11A
XLATED DATA 2**-10		•A05 10A, A07 10A
XLATED DATA 2**-11		•A05 09A, A07 09A
XLATED DATA 2**-12		•A05 08A, A07 08A
XLATED DATA 2**-13		•A05 07A, A07 07A
XLATOR A	*	•A05 28A, A08 30A
XLATOR B	*	A04 26A, •A05 26A
XLATOR OVERLOAD A	*	•A05 39A, A08 56A
XLATOR OVERLOAD B	*	•A05 40A, A08 55A
XLATOR READY		•A05 27A, A07 21A
Z/+N/+Z/-N/ 2**0		•A04 51B, A05 51B
Z/+N/+Z/-N/ 2**1		•A04 52B, A05 52B
Z/+N/+Z/-N/ 2**10		•A04 61B, A05 61B
Z/+N/+Z/-N/ 2**11		•A04 62B, A05 62B
Z/+N/+Z/-N/ 2**12		•A04 63B, A05 63B
Z/+N/+Z/-N/ 2**13		•A04 64B, A05 64B
Z/+N/+Z/-N/ 2**14		•A04 65B, A05 65B
Z/+N/+Z/-N/ 2**15		•A04 66B, A05 66B
Z/+N/+Z/-N/ 2**2		•A04 53B, A05 53B
Z/+N/+Z/-N/ 2**3		•A04 54B, A05 54B
Z/+N/+Z/-N/ 2**4		•A04 55B, A05 55B
Z/+N/+Z/-N/ 2**5		•A04 56B, A05 56B
Z/+N/+Z/-N/ 2**6		•A04 57B, A05 57B
Z/+N/+Z/-N/ 2**7		•A04 58B, A05 58B
Z/+N/+Z/-N/ 2**8		•A04 59B, A05 59B
Z/+N/+Z/-N/ 2**9		•A04 60B, A05 60B
ZERO OR NOT CARRY		A11 29A, •A12 32A
Z80 ADDR A00		A06 51B, A07 51B, •A08 51B, A09 51B, A16 51B, A17 51B, A18 93
Z80 ADDR A01		A06 52B, A07 52B, •A08 52B, A09 52B, A16 52B, A17 52B, A18 94
Z80 ADDR A02		A06 53B, A07 53B, •A08 53B, A09 53B, A16 53B, A17 53B, A18 91
Z80 ADDR A03		A06 54B, A07 54B, •A08 54B, A09 54B, A16 54B, A17 54B, A18 92
Z80 ADDR A04		A06 55B, A07 55B, •A08 55B, A09 55B, A16 55B, A17 55B, A18 89
Z80 ADDR A05		A06 56B, A07 56B, •A08 56B, A09 56B, A16 56B, A17 56B, A18 90
Z80 ADDR A06		A06 57B, A07 57B, •A08 57B, A09 57B, A16 57B, A17 57B, A18 87
Z80 ADDR A07		A08 58B, A09 58B, •A16 58B, A17 58B

I----SIGNAL NAME----I		I----------STRING LIST CONNECTOR / PIN----------I
Z80 ADDR A08		•A08 59B, A09 59B, A16 59B, A17 59B
Z80 ADDR A09		•A08 60B, A09 60B, A16 60B, A17 60B
Z80 ADDR A10		•A08 61B, A09 61B, A16 61B, A17 61B
Z80 ADDR A11		•A08 62B, A09 62B, A16 62B, A17 62B
Z80 ADDR A12		•A08 63B, A09 63B, A16 63B, A17 63B
Z80 ADDR A13		•A08 64B, A09 64B, A16 64B, A17 64B
Z80 ADDR A14		•A08 65B, A09 65B, A16 65B, A17 65B
Z80 ADDR A15		•A08 66B, A09 66B, A16 66B, A17 66B
Z80 CLK		•A06 03B, A08 04B, A09 04B
Z80 DATA D00		A03 35B, A04 35B, A05 35B, A06 35B, A07 35B, •A08 35B, A09 35B, A10 35B,
		A11 35B, A12 35B, A13 35B, A14 35B, A15 35B, A16 35B, A17 35B, A18 31
Z80 DATA D01		A03 36B, A04 36B, A05 36B, A06 36B, A07 36B, •A08 36B, A09 36B, A10 36B,
		A11 36B, A12 36B, A13 36B, A14 36B, A15 36B, A16 36B, A17 36B, A18 32
Z80 DATA D02		A03 37B, A04 37B, A05 37B, A06 37B, A07 37B, •A08 37B, A09 37B, A10 37B,
		A11 37B, A12 37B, A13 37B, A14 37B, A15 37B, A16 37B, A17 37B, A18 29
Z80 DATA D03		A03 38B, A04 38B, A05 38B, A06 38B, A07 38B, •A08 38B, A09 38B, A10 38B,
		A11 38B, A12 38B, A13 38B, A14 38B, A15 38B, A16 38B, A17 38B, A18 30
Z80 DATA D04		A03 39B, A04 39B, A05 39B, A06 39B, A07 39B, •A08 39B, A09 39B, A10 39B,
		A11 39B, A12 39B, A13 39B, A14 39B, A15 39B, A16 39B, A17 39B, A18 27
Z80 DATA D05		A03 40B, A04 40B, A05 40B, A06 40B, A07 40B, •A08 40B, A09 40B, A10 40B,
		A11 40B, A12 40B, A13 40B, A14 40B, A15 40B, A16 40B, A17 40B, A18 28
Z80 DATA D06		A03 41B, A04 41B, A05 41B, A06 41B, A07 41B, •A08 41B, A09 41B, A10 41B,
		A11 41B, A12 41B, A13 41B, A14 41B, A15 41B, A16 41B, A17 41B, A18 25
Z80 DATA D07		A03 42B, A04 42B, A05 42B, A06 42B, A07 42B, •A08 42B, A09 42B, A10 42B,
		A11 42B, A12 42B, A13 42B, A14 42B, A15 42B, A16 42B, A17 42B, A18 26
Z80 DATA D08		A03 43B, A04 43B, A05 43B, A06 43B, A07 43B, •A08 43B, A09 43B, A10 43B,
		A11 43B, A12 43B, A13 43B, A14 43B, A15 43B, A16 43B, A17 43B, A18 23
Z80 DATA D09		A03 44B, A04 44B, A05 44B, A06 44B, A07 44B, •A08 44B, A09 44B, A10 44B,
		A11 44B, A12 44B, A13 44B, A14 44B, A15 44B, A16 44B, A17 44B, A18 24
Z80 DATA D10		A03 45B, A04 45B, A05 45B, A06 45B, A07 45B, •A08 45B, A09 45B, A10 45B,
		A11 45B, A12 45B, A13 45B, A14 45B, A15 45B, A16 45B, A17 45B, A18 21
Z80 DATA D11		A03 46B, A04 46B, A05 46B, A06 46B, A07 46B, •A08 46B, A09 46B, A10 46B,
		A11 46B, A12 46B, A13 46B, A14 46B, A15 46B, A16 46B, A17 46B, A18 22
Z80 DATA D12		A03 47B, A05 47B, A06 47B, A07 47B, •A08 47B, A09 47B, A10 47B, A11 47B,
		A12 47B, A13 47B, A14 47B, A15 47B, A16 47B, A17 47B, A18 19
Z80 DATA D13		A03 48B, A05 48B, A06 48B, A07 48B, •A08 48B, A09 48B, A10 48B, A11 48B,
		A12 48B, A13 48B, A14 48B, A15 48B, A16 48B, A17 48B, A18 20
Z80 DATA D14		A03 49B, A05 49B, A06 49B, A07 49B, •A08 49B, A09 49B, A10 49B, A11 49B,
		A12 49B, A13 49B, A14 49B, A15 49B, A16 49B, A17 49B, A18 17
Z80 DATA D15		A03 50B, A05 50B, A06 50B, A07 50B, •A08 50B, A09 50B, A10 50B, A11 50B,
		A12 50B, A13 50B, A14 50B, A15 50B, A16 50B, A17 50B, A18 18
Z80 DATA INPUT	*P	•A06 66B, A07 66B
Z80 I/O READ	*P	•A08 14B, A09 14B, A12 04B, A13 04B, A14 04B, A17 04B, A18103
Z80 I/O WRITE	*P	A03 15B, A04 15B, •A08 13B, A09 13B, A12 03B, A14 03B, A16 03B, A17 03B
Z80 MEM READ	*P	A06 16B, A07 16B, •A08 16B, A09 16B, A17 08B
Z80 MEM WRITE	*P	A06 15B, A07 15B, •A08 15B, A09 15B, A16 04B, A17 07B
Z80 TK CAPT TRIG	*P	A06 36A, •A08 36A
0.1 FS A		•A01 63B, A18141
0.1 FS B		•A02 63B, A18143

SIGNAL NAME	STRING LIST CONNECTOR / PIN
0.5 F.S. A	•A01 65B, A18142
0.5 F.S. B	•A02 65B, A18144
03	A04 13B, •A05 13B
04	A04 14B, •A05 14B
1KHZ CLK	•A06 93A
10 HZ CLK	•A06 97A, A14 97A, A15 97A
16.384 MHZ CLK	A01 04B, A02 04B, A03 04B, A05 04B, •A06 04B, A07 04B, A10 04B, A12 93A, A14 93A
2 MHZ CLK	A01 98A, A02 98A, A03 98A, •A06 98A
20.48 KHZ CLK	•A06 44A
3000 ACCESS EN	A11 08A, •A14 08A
3000 ADDR A00	A09 51A, •A12 51A, A13 51A, A14 51A, A15 51A, A16 51A, A17 51A
3000 ADDR A01	A09 52A, •A12 52A, A13 52A, A14 52A, A15 52A, A16 52A, A17 52A
3000 ADDR A02	A09 53A, •A12 53A, A13 53A, A14 53A, A15 53A, A16 53A, A17 53A
3000 ADDR A03	A09 54A, •A12 54A, A13 54A, A14 54A, A15 54A, A16 54A, A17 54A
3000 ADDR A04	A09 55A, •A12 55A, A13 55A, A14 55A, A15 55A, A16 55A, A17 55A
3000 ADDR A05	A09 56A, •A12 56A, A13 56A, A14 56A, A15 56A, A16 56A, A17 56A
3000 ADDR A06	A09 61A, •A12 57A, A13 57A, A14 57A, A15 57A, A16 57A, A17 57A
3000 ADDR A07	A09 62A, •A12 58A, A13 58A, A14 58A, A15 58A, A16 58A, A17 58A
3000 ADDR A08	A09 59A, •A12 59A, A13 59A, A14 59A, A15 59A, A16 59A, A17 59A
3000 ADDR A09	A09 64A, •A12 60A, A13 60A, A14 60A, A15 60A, A16 60A, A17 60A
3000 ADDR A10	•A12 61A, A13 61A, A14 61A, A15 61A, A16 61A, A17 61A
3000 ADDR A11	•A12 62A, A13 62A, A14 62A, A15 62A, A16 62A, A17 62A
3000 ADDR A12	•A12 63A, A13 63A, A14 63A, A15 63A, A16 63A, A17 63A
3000 ADDR A13	•A12 64A, A13 64A, A14 64A, A15 64A, A16 64A, A17 64A
3000 ADDR A14	•A12 65A, A13 65A, A14 65A, A15 65A, A16 65A, A17 65A
3000 ADDR A15	•A12 66A, A13 66A, A14 66A, A15 66A, A16 66A, A17 66A
3000 ADDR SW SEL *	A12 59B, •A13 62B
3000 D BUS SIGN	A07 86A, A08 86A, A09 86A, A10 86A, A11 86A, •A12 86A, A13 86A, A14 86A, A15 86A, A16 86A, A17 86A, A18127
3000 D BUS 2** 00	A07 84A, A08 84A, A09 84A, A10 84A, A11 84A, •A12 84A, A13 84A, A14 84A, A15 84A, A16 84A, A17 84A, A18125
3000 D BUS 2** 01	A07 85A, A08 85A, A09 85A, A10 85A, A11 85A, •A12 85A, A13 85A, A14 85A, A15 85A, A16 85A, A17 85A, A18128
3000 D BUS 2**-01	A07 83A, A08 83A, A09 83A, A10 83A, A11 83A, •A12 83A, A13 83A, A14 83A, A15 83A, A16 83A, A17 83A, A18126
3000 D BUS 2**-02	A07 82A, A08 82A, A09 82A, A10 82A, A11 82A, •A12 82A, A13 82A, A14 82A, A15 82A, A16 82A, A17 82A, A18123
3000 D BUS 2**-03	A07 81A, A08 81A, A09 81A, A10 81A, A11 81A, •A12 81A, A13 81A, A14 81A, A15 81A, A16 81A, A17 81A, A18124
3000 D BUS 2**-04	A07 80A, A08 80A, A09 80A, A10 80A, A11 80A, •A12 80A, A13 80A, A14 80A, A15 80A, A16 80A, A17 80A, A18121
3000 D BUS 2**-05	A07 79A, A08 79A, A09 79A, A10 79A, A11 79A, •A12 79A, A13 79A, A14 79A, A15 79A, A16 79A, A17 79A, A18122
3000 D BUS 2**-06	A07 78A, A08 78A, A09 78A, A10 78A, A11 78A, •A12 78A, A13 78A, A14 78A, A15 78A, A16 78A, A17 78A, A18119
3000 D BUS 2**-07	A07 77A, A08 77A, A09 77A, A10 77A, A11 77A, •A12 77A, A13 77A, A14 77A, A15 77A, A16 77A, A17 77A, A18120
3000 D BUS 2**-08	A07 76A, A08 76A, A09 76A, A10 76A, A11 76A, •A12 76A, A13 76A, A14 76A,

SIGNAL NAME		STRING LIST CONNECTOR / PIN
		A15 76A, A16 76A, A17 76A, A18117
3000 D BUS 2**-09		A07 75A, A08 75A, A09 75A, A10 75A, A11 75A, •A12 75A, A13 75A, A14 75A,
		A15 75A, A16 75A, A17 75A, A18118
3000 D BUS 2**-10		A07 74A, A08 74A, A09 74A, A10 74A, A11 74A, •A12 74A, A13 74A, A14 74A,
		A15 74A, A16 74A, A17 74A, A18115
3000 D BUS 2**-11		A07 73A, A08 73A, A09 73A, A10 73A, A11 73A, •A12 73A, A13 73A, A14 73A,
		A15 73A, A16 73A, A17 73A, A18116
3000 D BUS 2**-12		A07 72A, A08 72A, A09 72A, A10 72A, A11 72A, •A12 72A, A13 72A, A14 72A,
		A15 72A, A16 72A, A17 72A, A18113
3000 D BUS 2**-13		A07 71A, A08 71A, A09 71A, A10 71A, A11 71A, •A12 71A, A13 71A, A14 71A,
		A15 71A, A16 71A, A17 71A, A18114
3000 MEM WRITE	*P	A09 63A, •A12 49A, A13 49A, A14 49A, A18104
3000 REQUEST	*P	•A12 11A, A14 11A
80 HZ CLK		•A06 43A, A08 94A, A15 98A

APPENDIX C
TYPE N3002 CENTRAL PROCESSING ELEMENT (CPE)
(From Signetics Corp. Data Sheets)

DESCRIPTION

The N3002 Central Processing Element (CPE) is one part of a bipolar microcomputer set. The N3002 is organized as a 2-bit slice and performs the logical and arithmetic functions required by microinstructions. A system with any number of bits in a data word can be implemented by using multiple N3002s, the N3001 microcomputer control unit, the N74S182 carry look-ahead unit and ROM or PROM memory.

FEATURES

- 45ns cycle time (typ)
- Easy expansion to multiple of 2 bits
- 11 general purpose registers
- Full function accumulator
- Useful functions include:
  - 2's complement arithmetic
  - Logical AND, OR, NOT, exclusive-NOR
  - Increment, decrement
  - Shift left/shift right
  - Bit testing and zero detection
  - Carry look-ahead generation
  - Masking via K-bus
  - Conditioned clocking allowing non-destructive testing of data in accumulator and scratchpad
- 3 input buses
- 2 output buses
- Control bus

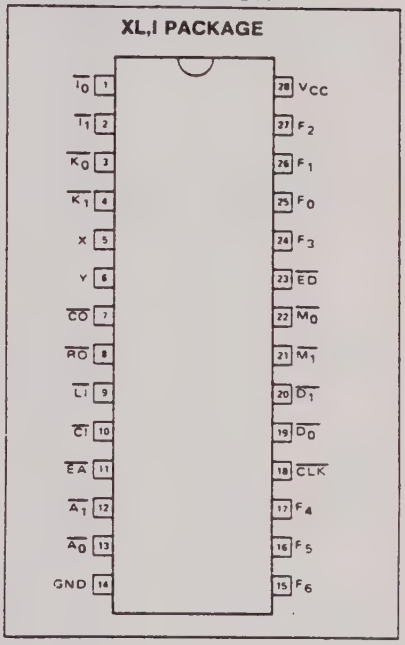
FUNCTION TRUTH TABLE

FUNCTION GROUP	F_6	F_5	F_4
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

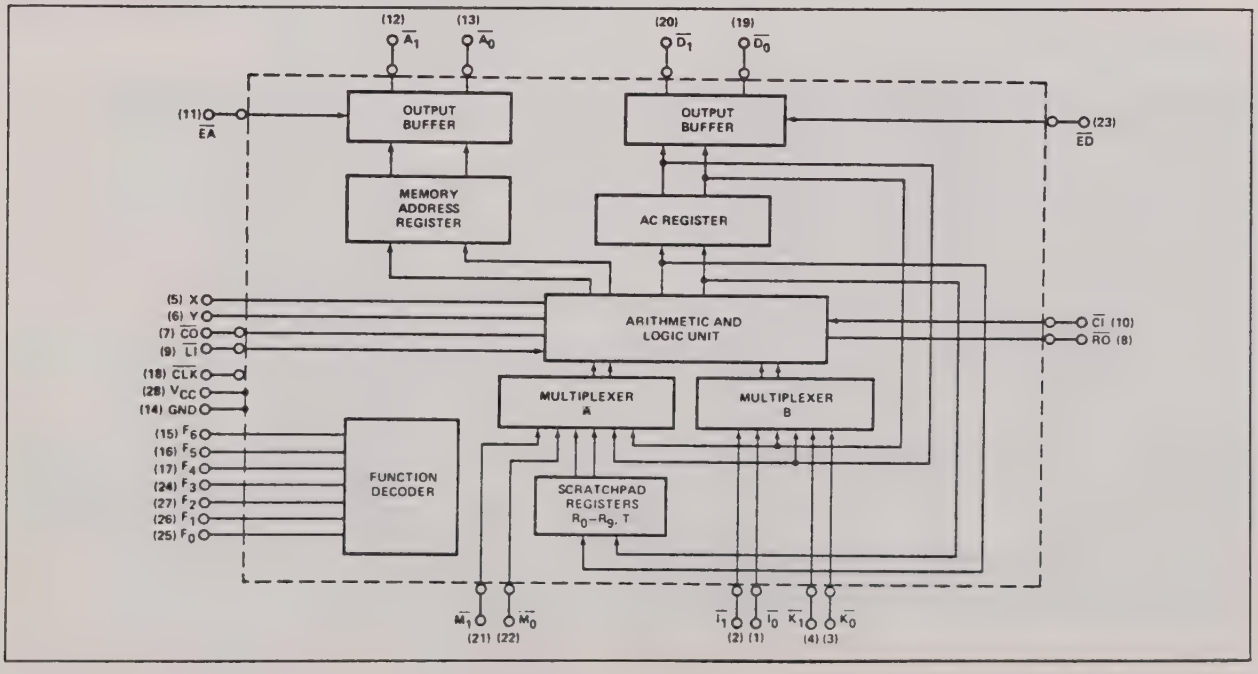
REGISTER GROUP	REGISTER	F_3	F_2	F_1	F_0
I	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
II	T	1	0	1	0
	AC	1	0	1	1
III	T	1	1	1.	0
	AC	1	1	1	1

PIN CONFIGURATION

XL,I PACKAGE



BLOCK DIAGRAM



PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
1, 2	$\overline{I_0}$-$\overline{I_1}$	External Bus Inputs The external bus inputs provide a separate input port for external input devices.	Active low
3, 4	$\overline{K_0}$-$\overline{K_1}$	Mask Bus Inputs The mask bus inputs provide a separate input port from the microprogram memory, to allow mask or constant entry.	Active low
5, 6	X, Y	Standard Carry Look-Ahead Cascade Outputs The cascade outputs allow high speed arithmetic operations to be performed when they are used in conjunction with the 74S182 Look-Ahead Carry Generator	Active high
7	$\overline{CO}$	Ripple Carry Out The ripple carry output is only disabled during shift right operations.	Active low Three-state
8	$\overline{RO}$	Shift Right Output The shift right output is only enabled during shift right operations.	Active low Three-state
9	$\overline{LI}$	Shift Right Input	Active low
10	$\overline{CI}$	Carry Input	Active low
11	$\overline{EA}$	Memory Address Enable Input When in the low state, the memory address enable input enables the memory address outputs (A_0-A_1).	Active low
12-13	$\overline{A_0}$-$\overline{A_1}$	Memory Address Bus Outputs The memory address bus outputs are the buffered outputs of the memory address register (MAR).	Active low Three-state
14	GND	Ground	
14-17, 24-27	F_0-F_6	Micro-Function Bus Inputs The micro-function bus inputs control ALU function and register selection.	Active high
18	$\overline{CLK}$	Clock Input	
19-20	$\overline{D_0}$-$\overline{D_1}$	Memory Data Bus Outputs The memory data bus outputs are the buffered outputs of the full function accumulator register (AC).	Active low Three-state
21-22	$\overline{M_0}$-$\overline{M_1}$	Memory Data Bus Inputs The memory data bus inputs provide a separate input port for memory data.	Active low
23	$\overline{ED}$	Memory Data Enable Input When in the low state, the memory data enable input enables the memory data outputs (D_0-D_1).	Active low
28	V_{CC}	+5 Volt Supply	

SYSTEM DESCRIPTION

Microfunction Decoder and K-Bus

Basic microfunctions are controlled by a 7-bit bus (F_0-F_6) which is organized into 2 groups. The higher 3 bits (F_4-F_6) are designated as F-Group and the lower 4 bits (F_0-F_3) are designated as the R-Group. The F-Group specifies the type of operation to be performed and the R-Group specifies the registers involved.

The F-Bus instructs the microfunction decoder to:
- Select ALU functions to be performed
- Generate scratchpad register address
- Control A and B multiplexer

The resulting microfunction action can be:
- Data transfer
- Shift operations
- Increment and decrement
- Initialize stack
- Test for zero conditions
- 2's complement addition and subtraction
- Bit masking
- Maintain program counter

A and B Multiplexers

A and B multiplexers select the proper 2 operands to the ALU.

A multiplexer selects inputs from one of the following:
- M-bus (data from main memory)
- Scratchpad registers
- Accumulator

B multiplexer selects inputs from one of the following:
- I-bus (data from external I/O devices)
- Accumulator
- K-bus (literal or masking information from micro-program memory)

Scratchpad Registers

- Contains 11 registers (R_0-R_9, $\overline{T}$)
- Scratchpad register outputs are multiplexed to the ALU via the A multiplexer
- Used to store intermediate results from arithmetic/logic operations
- Can be used as program counter

Arithmetic/Logic Unit (ALU)

The ALU performs the arithmetic and logic operations of the CPE.

Arithmetic operations are:
- 2's complement addition
- Incrementing
- Decrementing
- Shift left
- Shift right

Logical operations are:
- Transfer
- AND
- Inclusive-OR
- Exclusive-NOR
- Logic complement

ALU operation results are then stored in the accumulator and/or scratchpad registers. For easy expansion to larger arrays, carry look-ahead outputs (X and Y) and cascading shift inputs (LI, RO) are provided.

Accumulator

- Stores results from ALU operations
- The output of accumulator is multiplexed into ALU via the A and B multiplexer as one of the operands

Input Buses

M-bus: Data bus from main memory

- Accepts 2 bits of data from main memory into CPE
- Is multiplexed into the ALU via the A multiplexer

I-bus: Data bus from input/output devices

- Accepts 2 bits of data from external input/output devices into CPE
- Is multiplexed into the ALU via the B multiplexer

K-bus: A special feature of the N3002 CPE

- During arithmetic operations, the K-bus can be used to **mask** portions of the field being operated on
- Select or remove accumulator from operation by placing K-bus in all "1" or all "0" state respectively
- During non-arithmetic operation, the carry circuit can be used in conjunction with the K-bus for word-wise-OR operation for bit testing
- Supply literal or constant data to CPE

Output Buses

A-bus and Memory Address Register

- Main memory address is stored in the memory address register (MAR)
- Main memory is addressed via the A-bus
- MAR and A-bus may also be used to generate device address when executing I/OO instruc-instructions
- A-bus has Tri-State outputs

D-bus: Data bus from CPE to main memory or to I/O devices

- Sends buffered accumulator outputs to main memory or the external I/O devices
- D-bus has Tri-State outputs

FUNCTION DESCRIPTION

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
0	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n, AC$	**Logically AND AC with the K-bus.** Add the result to R_n and carry input (CI). Deposit the sum in AC and R_n.
		OO	ILR	$R_n + CI \rightarrow R\ , AC$	Conditionally increment R_n and load the result in AC. Used to load AC from R_n or to increment R_n and load a copy of the result in AC.
		11	ALR	$AC + R_n + CI \rightarrow R_n, AC$	Add AC and CI to R_n and load the result in AC. Used to add AC to a register. If R_n is AC, then AC is shifted left one bit position.
0	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.
0	III	XX	—	$AT_L \wedge (\overline{I_L \wedge K_L}) \rightarrow RO$ $LI \vee [(I_H \wedge K_H) \wedge AT_H] \rightarrow AT_H$ $[AT_L \wedge (I_L \wedge K_L)]$ $[AT_H \vee (I_H \wedge K_H)] \rightarrow AT_L$	None
		OO	SRA	$AT_L \rightarrow RO$ $AT_H \rightarrow AT_L$ $LI \rightarrow AT_H$	Shift AC or T, as specified, right one bit position. Place the previous low order bit value on RO and fill the high order bit from the data on LI. Used to shift or rotate AC or T right one bit.
1	I	XX	—	$K \vee R_n \rightarrow MAR$ $R_n + K + CI \rightarrow R_n$	**Logically OR R_n with the K-bus.** Deposit the result in MAR. Add the K-bus to Rn and CI. Deposit the result in R_n.
		OO	LMI	$Rn \rightarrow MAR,\ Rn + CI \rightarrow Rn$	Load MAR from R_n. Conditionally increment R_n. Used to maintain a macro-instruction program counter.
		11	DSM	$11 \rightarrow MAR,\ Rn - 1 + CI \rightarrow Rn$	Set MAR to all ones. Conditionally decrement R_n by one. Used to force MAR to its highest address and to decrement Rn.
1	II	XX	—	$KVM \rightarrow MAR$ $M + K + CI \rightarrow AT$	**Logically OR the M-bus with the K-Bus.** Deposit the result in MAR. Add the K-bus to the M-bus and CI. Deposit the sum in AC or T.
		OO	LMM	$M \rightarrow MAR,\ M + CI \rightarrow AT$	Load MAR from the M-bus. Add CI to the M-bus. Deposit the result in AC or T. Used to load the address register with memory data for macro-instructions using indirect addressing.
		11	LDM	$11 \rightarrow MAR$ $M - 1 + CI \rightarrow AT$	Set MAR to all ones. Subtract one from the M-bus. Add CI to the difference and deposit the result in AC or T, as specified. Used to load decremented memory data in AC or T.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
1	III	XX	—	$(\overline{AT} \vee K) + (AT \wedge K) + CI \rightarrow AT$	**Logically OR the K-bus with the complement of AC or T, as specified.** Add the result to the logical AND of specified register with the K-bus. Add the sum to CI. Deposit the result in the specified register.
		OO	CIA	$\overline{AT} + CI \rightarrow AT$	Add CI to the complement of AC or T, as specified. Deposit the result in the specified register. Used to form the 1's or 2's complement of AC or T.
		11	DCA	$\overline{AT} - 1 + CI \rightarrow AT$	Subtract one from AC or T, as specified. Add CI to the difference and deposit the sum in the specified register. Used to decrement AC or T.
2	I	XX	—	$(AC \wedge K) - 1 + CI \rightarrow R_n$	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in R_n.
		OO	CSR	$CI - 1 \rightarrow R_n$ (See Note 1)	Subtract one from CI and deposit the difference in Rn. Used to conditionally clear or set R_n to all 0's or 1's, respectively.
		11	SDR	$AC - 1 + CI \rightarrow R_n$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in R_n. Used to store AC in R_n or to store the decremented value of AC in R_n.
2	II	XX	—	$(AC \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the K-bus with AC.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$ (See Note 1)	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	SDA	$AC - 1 + CI \rightarrow AT$ (See Note 1)	Subtract one from AC and add the difference to CI. Deposit the sum in AC or T. Used to store AC in T, or decrement AC, or store the decremented value of AC in T.
2	III	XX	—	$(I \wedge K) - 1 + CI \rightarrow AT$ (See Note 1)	**Logically AND the data of the K-bus with the data on the I-bus.** Subtract one from the result and add the difference to CI. Deposit the sum in AC or T, as specified.
		OO	CSA	$CI - 1 \rightarrow AT$	Subtract one from CI and deposit the difference in AC or T. Used to conditionally clear or set AC or T.
		11	LDI	$I - 1 + CI \rightarrow AT$	Subtract one from the data on the I-bus and add the difference to CI. Deposit the sum in AC or T, as specified. Used to load input bus data or decremented input bus data in the specified register.
3	I	XX	—	$R_n + (AC \wedge K) + CI \rightarrow R_n$	**Logically AND AC with the K-bus.** Add R_n and CI to the result. Deposit the sum in R_n.
		OO	INR	$R_n + CI \rightarrow R_n$	Add CI to R_n and deposit the sum in R_n. Used to increment R_n.
		11	ADR	$AC + R_n + CI \rightarrow R_n$	Add AC to R_n. Add the result to CI and deposit the sum in R_n. Used to add the accumulator to a register or to add the incremented value of the accumulator to a register.
3	II	XX	—	$M + (AC \wedge K) + CI \rightarrow AT$	**Logically AND AC with the K-bus.** Add the result to CI and the M-bus. Deposit the sum in AC or T.
		OO	ACM	$M + CI \rightarrow AT$	Add CI to M-bus. Load the result in AC or T, as specified. Used to load memory data in the specified register, or to load incremented memory data in the specified register.
		11	AMA	$M + AC + CI \rightarrow AT$	Add the M-bus to AC and CI, and load the result in AC or T, as specified. Used to add memory data or incremented memory data to AC and store the sum in the specified register.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
3	III	XX	—	AT + (I ∧ K) + CI → AT	**Logically AND the K-bus with the I-bus.** Add CI and the contents of AC or T, as specified, to the result. Deposit the sum in the specified register.
		OO	INA	AT + CI → AT	Conditionally increment AC or T. Used to increment AC or T.
		11	AIA	I + AT + CI → AT	Add the I-bus to AC or T. Add CI to the result and deposit the sum in the specified register. Used to add input data or incremented input data to the specified register.
4	I	XX	—	CI ∨ (R_n ∧ AC ∧ K) → CO R_n ∧ (AC ∧ K) → R_n	**Logically AND the K-bus with AC.** Logically AND the result with the contents of R_n. Deposit the final result in R_n. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on the carry output (CO) line.
		OO	CLR	CI → CO, O → R_n	Clear R_n to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	ANR	CI ∨ (R_n ∧ AC) → CO R_n ∧ AC → R_n	Logically AND AC with R_n. Deposit the result in R_n. Force CO to one if the result is non-zero. Used to AND the accumulator with a register and test for a zero result.
4	II	XX	—	CI ∨ (M ∧ AC ∧ K) → CO M ∧ (AC ∧ K) → AT	**Logically AND the K-bus with AC.** Logically AND the result with the M-bus. Deposit the final result in AC or T. Logically OR the value of CI with the word-wise OR of the bits of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANM	CI ∨ (M ∧ AC) → CO M ∧ AC → AT	Logically AND the M-bus with AC. Deposit the result in AC or T. Force CO to one if the result is non-zero. Used to AND M-bus data to the accumulator and test for a zero result.
4	III	XX	—	CI ∨ (AT ∧ 1 ∧ K) → CO AT ∧ (I ∧ K) → AT	**Logically AND the I-bus with the K-bus.** Logically AND the result with AC or T. Deposit the final result in the specified register. Logically OR CI with the word-wise OR of the final result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	ANI	CI ∨ (AT ∧ I) → CO AT ∧ 1 → AT	Logically AND the I-bus with AC or T, as specified. Deposit the result in the specified register. Force CO to one if the result is non-zero. Used to AND the I-bus to the accumulator and test for a zero result.
5	I	XX	—	CI ∨ (R_n ∧ K) → CO K ∧ R_n → R_n	**Logically AND the K-bus with R_n.** Deposit the result in Rn. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLR	CI → CO, O → R_n	Clear Rn to all O's. Force CO to CI. Used to clear a register and force CO to CI.
		11	TZR	CI ∨ R_n → CO R_n → R_n	Force CO to one if Rn is non-zero. Used to test a register for zero. Also used to AND K-bus data with a register for masking and, optionally, testing for a zero result.
5	II	XX	—	CI ∨ (M ∧ K) → CO K ∧ M → AT	**Logically AND the K-bus with the M-bus.** Deposit the result in AC or T, as specified. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, O → AT	Clear AC or T, as specified, to all O's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	LTM	CI ∨ M → CO M → AT	Load AC or T, as specified, from the M-bus. Force CO to one if the result is non-zero. Used to load the specified register from memory and test for a zero result. Also used to AND the K-bus with the M-bus for masking and, optionally, testing for a zero result.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
5	III	XX	—	CI ∨ (AT ∧ K) → CO K ∧ AT → AT	Logically AND the K-bus with AC or T, as specified. Deposit the result in the specified register. Logically OR CI with the word-wise OR of the result. Place the value of the carry OR on CO.
		OO	CLA	CI → CO, 0 → AT	Clear AC or T, as specified, to all 0's. Force CO to CI. Used to clear the specified register and force CO to CI.
		11	TZA	CI ∨ AT → CO AT → AT	Force CO to one if AC or T, as specified, is non-zero. Used to test the specified register for zero. Also used to AND the K-bus to the specified register for masking and, optionally, testing for a zero result.
6	I	XX	—	CI ∨ (AC ∧ K) → CO R_n ∨ (AC ∧ K) → R_n	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the result of the carry OR on CO. Logically OR R_n with the logical AND of AC and the K-bus. Deposit the result in R_n.
		OO	NOP	CI → CO, R_n → R_n	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORR	CI ∨ AC → CO R_n ∨ AC → R_n	Force CO to one if AC is non-zero. Logically OR AC with R_n. Deposit the result in R_n. Used to OR the accumulator to a register and, optionally, test the previous accumulator value for zero.
6	II	XX	—	CI ∨ (AC ∧ K) → CO M ∨ (AC ∧ K) → AT	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus. Place the carry OR on CO. Logically OR the M-bus, with the logical AND of AC and the K-bus. Deposit the final result in AC or T.
		OO	LMF	CI → CO, M → AT	Load AC or T, as specified, from the M-bus. Force CO to CI. Used to load the specified register with memory data and force CO to CI.
		11	ORM	CI ∨ AC → CO M ∨ AC → AT	Force CO to one if AC is non-zero. Logically OR the M-bus with AC. Deposit the result in AC or T, as specified. Used to OR M-bus with the AC and, optionally, test the previous value of AC for zero.
6	III	XX	—	CI ∨ (I ∧ K) → CO AT ∨ (I ∧ I) → AT	Logical OR CI with the word-wise OR of the logical AND of the I-bus and the K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Logically OR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	NOP	CI → CO, AT → AT	Force CO to CI. Used as a null operation or to force CO to CI.
		11	ORI	CI ∨ I → CO I ∨ AT → AT	Force CO to one if the data on the I-bus is non-zero. Logically OR the I-bus to AC or T, as specified. Deposit the result in the specified register. Used to OR I-bus data with the specified register and, optionally, test the I-bus data for zero.
7	I	XX	—	CI ∨ (R_n ∧ AC ∧ K) → CO R_n ⊕̄ (AC ∧ K) → R_n	Logically OR CI with the word-wise OR of the logical AND of R_n and AC and the K-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive-NOR the result with R_n. Deposit the final result in R_n.
		OO	CMR	CI → CO, Rn → Rn	Complement the contents of R_n. Force CO to CI.
		11	XNR	CI ∨ (R_n ∧ AC) → CO R_n ⊕̄ AC → R_n	Force CO to one if the logical AND of AC and Rn is non-zero. Exclusive-NOR AC with R_n. Deposit the result in R_n. Used to exclusive-NOR the accumulator with a register.

FUNCTION DESCRIPTION (Cont'd)

F GROUP	R GROUP	K BUS	NAME	EQUATION	DESCRIPTION
7	II	XX	—	$CI \vee (M \wedge AC \wedge K) \rightarrow CO$ $M \overline{\oplus} (AC \wedge K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of AC and the K-bus and M-bus. Place the carry OR on CO. Logically AND the K-bus with AC. Exclusive NOR the result with the M-bus. Deposit the final result in AC or T.
		OO	LCM	$CI \rightarrow CO, \overline{M} \rightarrow AT$	Load the complement of the M-bus into AC or T, as specified. Force CO to CI.
		11	XNM	$CI \vee (M \wedge AC) \rightarrow CO$ $M \overline{\oplus} AC \rightarrow AT$	Force CO to one if the logical AND of AC and the M-bus is non-zero. Exclusive-NOR AC with the M-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR memory data with the accumulator.
7	III	XX	—	$CI \vee (AT \wedge I \wedge K) \rightarrow CO$ $AT \overline{\oplus} (I \quad K) \rightarrow AT$	Logically OR CI with the word-wise OR of the logical AND of the specified register and the I-bus and K-bus. Place the carry OR on CO. Logically AND the K-bus with the I-bus. Exclusive-NOR the result with AC or T, as specified. Deposit the final result in the specified register.
		OO	CMA	$CI \rightarrow CO, \overline{AT} \rightarrow AT$	Complement AC or T, as specified. Force CO to CI.
		11	XNI	$CI \vee (AT \wedge I) \rightarrow CO$ $I \overline{\oplus} AT \rightarrow AT$	Force CO to one if the logical AND of the specified register and the I-bus is non-zero. Exclusive-NOR AC with the I-bus. Deposit the result in AC or T, as specified. Used to exclusive-NOR input data with the accumulator.

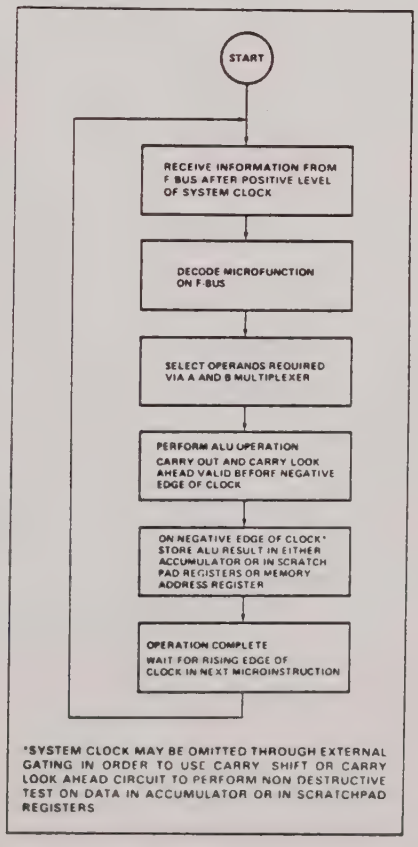
FUNCTION DESCRIPTION KEY

SYMBOL	MEANING
I,K,M	Data on the I, K, and M buses, respectively
CI,LI	Data on the carry input and left input, respectively
CO,RO	Data on the carry output and right output, respectively
Rn	Contents of register n including T and AC (R-Group I)
AC	Contents of the accumulator
AT	Contents of AC or T, as specified
MAR	Contents of the memory address register
L,H	As subscripts, designate low and high order bit, respectively
+	2's complement addition
-	2's complement subtraction
$\wedge$	Logical AND
$\vee$	Logical OR
$\oplus$	Exclusive-NOR
→	Deposit into

NOTE

1. 2's complement arithmetic adds 111 . . . 11 to perform subtraction of 000 . . . 01.

MICROCYCLE TIMING SEQUENCE

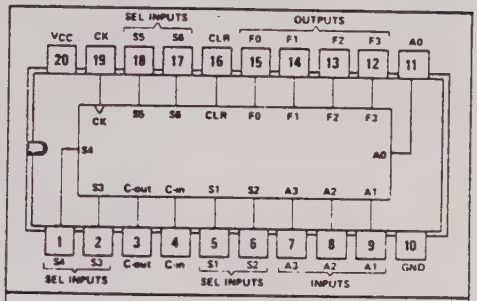

START
RECEIVE INFORMATION FROM F BUS AFTER POSITIVE LEVEL OF SYSTEM CLOCK
DECODE MICROFUNCTION ON F-BUS
SELECT OPERANDS REQUIRED VIA A AND B MULTIPLEXER
PERFORM ALU OPERATION
CARRY OUT AND CARRY LOOK AHEAD VALID BEFORE NEGATIVE EDGE OF CLOCK
ON NEGATIVE EDGE OF CLOCK* STORE ALU RESULT IN EITHER ACCUMULATOR OR IN SCRATCH PAD REGISTERS OR MEMORY ADDRESS REGISTER
OPERATION COMPLETE
WAIT FOR RISING EDGE OF CLOCK IN NEXT MICROINSTRUCTION

*SYSTEM CLOCK MAY BE OMITTED THROUGH EXTERNAL GATING IN ORDER TO USE CARRY SHIFT OR CARRY LOOK AHEAD CIRCUIT TO PERFORM NON DESTRUCTIVE TEST ON DATA IN ACCUMULATOR OR IN SCRATCHPAD REGISTERS

APPENDIX D
TYPE SN74S482N ADDRESS GENERATOR
(From Texas Instruments Inc. Data Sheets)

- 4-Bit Slice is Cascadable to N-Bits
- Designed Specifically for Microcontroller/ Next-Address Generator Functions
- Increment/Decrement by One (Immediate or Direct Symbolic Addressing Modes)
- Offset, Vector, or Branch (Indexed or Relative Addressing Modes)
- Store Up to Four Returns or Links (Program Return Address from Subroutine)
- Program Start or Initialize (Return to Zero or Clear Mode)
- On-Chip Edge-Triggered Output Register (Provides Steady-State Micro-Address/ Instruction)
- High-Density 20-Pin Dual-in-Line Package with 300-Mil Row Pin Spacing

SN54S482 . . . J PACKAGE
SN74S482 . . . J OR N PACKAGE
(TOP VIEW)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OUTPUTS
VCC CK S5 S6 CLR F0 F1 F2 F3 A0
20 19 18 17 16 15 14 13 12 11
S4 A0
S3 C-out C-in S1 S2 A3 A2 A1
1 2 3 4 5 6 7 8 9 10
SEL INPUTS
SEL INPUTS
INPUTS
GND

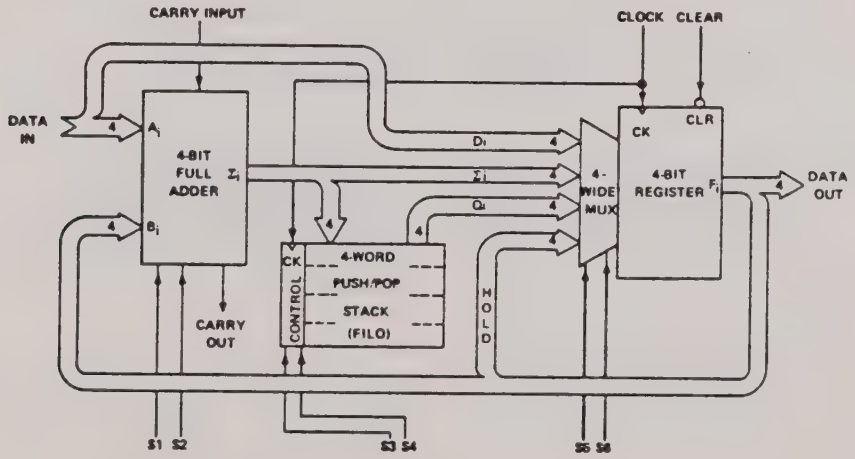
positive logic: See function table.

description

The 'S482 is a high-performance Schottky TTL 4-bit-slice control element for use in any computer/control application requiring the coupling of high-performance bipolar speeds with the flexibility of microprogram control and bit-slice expandability. When used as a next-address generator, two 'S482 elements can address up to 256 words of microprogram; three elements can addresss up to 4096 words of microprogram; or a number of 'S482 elements can generate N words in multiples of four lines.

Comprised of an output register, push-pop stack, and a full adder, the 'S482 provides the capability to implement multiway testing needed to generate or to determine and select the source of the next function of microprogram address.

functional block diagram



output register and source functions

The 4-bit edge-triggered register provides a steady-state output throughout each system clock cycle. An asynchronous clear extends the multiway testing to directly implement system initialization at ROM address zero.

Two source-select lines (S5, S6) provide the output register with access to either the current instruction (no change), an operand or address stored in the push-pop stack, the output of a four-function full adder, or a direct data-in address port. The sources and functions are summarized in Tables I and II.

TABLE I. REGISTER-SOURCE FUNCTIONS

SELECT		REGISTER INPUT SOURCE
S5	S6	
L	L	DATA-IN PORT (Di)
L	H	FULL ADDER OUTPUTS (Σi)
H	L	PUSH-POP STACK OUTPUTS (Qi)
H	H	REGISTER OUTPUTS (HOLD)

H ≡ high level, L ≡ low level

TABLE II. PUSH-POP STACK CONTROL AND REGISTER-SOURCE FUNCTIONS

	INPUTS						INTERNAL	OUTPUTS
	S3	S4	S5	S6	CLOCK	CLEAR	QiA	Fi
HOLD	X	X	X	X	L	H	QiA0	Fi0
CLEAR	X	X	X	X	X	L	QiA0	L
PUSH-POP STACK "HOLD"	L	L	L	L	↑	H	QiA0*	Di
	L	L	L	H	↑	H	QiA0*	Σi
	L	L	H	L	↑	H	QiA0*	QiA0
	L	L	H	H	↑	H	QiA0*	Fi0
PUSH-POP STACK "LOAD"	L	H	L	L	↑	H	Σi*	Di
	L	H	L	H	↑	H	Σi*	Σi
	L	H	H	L	↑	H	Σi*	QiA0
	L	H	H	H	↑	H	Σi*	Fi0
PUSH-POP STACK "POP"	H	L	L	L	↑	H	QiB0†	Di
	H	L	L	H	↑	H	QiB0†	Σi
	H	L	H	L	↑	H	QiB0†	QiA0
	H	L	H	H	↑	H	QiB0†	Fi0
PUSH-POP STACK "PUSH"	H	H	L	L	↑	H	Σi‡	Di
	H	H	L	H	↑	H	Σi‡	Σi
	H	H	H	L	↑	H	Σi‡	QiA0
	H	H	H	H	↑	H	Σi‡	Fi0

MSB LSB
i ≡ 3, 2, 1, 0
Ai ≡ Data inputs
QiA ≡ Push-pop stack word A output (internal)
QiA0 ≡ the level of Qi before the indicated inputs conditions were established.

Fi ≡ Device outputs
Fi0 ≡ the level of Fi before the indicated input conditions were established.
Σi ≡ Adder outputs (internal)
*QiB, QiC, QiD do not change
†QiD0 → QiD, QiD0 → QiC, QiC0 → QiB, QiB0 → QiA
‡QiA0 → QiB, QiB0 → QiC, QiC0 → QiD

push-pop stack control

The 4-word push-pop stack can be used for nesting up to four levels of program or return (link) addresses. In the load mode, the first (top) word is filled with new data from the output of the full adder, and no push occurs meaning that previous data at that location is lost. However, all other word locations in the push-pop stack remain unchanged. In the push mode, the new word is again entered in the first (top) location; however, previous data residing in the top three words are pushed down one word location and retained at their new locations. The bottom word is written over and lost.

In the pop mode, words in the push-pop stack move up one location on each clock transition. A unique function is provided by the bottom (fourth) register as its content is retained during the pop mode, and after 3 clock transitions, all words in the stack are filled with the operand/address that occupied the bottom register.

The operand/address will remain available indefinitely if stack functions are limited to the pop or hold modes.

The push-pop stack functions are shown in Tables II and III.

TABLE III. PUSH-POP STACK FUNCTIONS

	FUNCTION	SEL. S3	SEL. S4	REG. D	REG. C	REG. B	REG. A	INPUT/ OUTPUT
BIT 0	LOAD	L	H	QiD0	QiC0	QiB0	← Σi	Σi IN
BIT 1	PUSH	H	H	← QiC0	← QiB0	← QiA0	← Σi	Σi IN
BIT 2	POP	H	L	↶ → QiD0	→ QiD0	→ QiC0	→ QiB0	QiA OUT
BIT 3	HOLD	L	L	QiD0	QiC0	QiB0	QiA0	QiA OUT

*Link operations show previous data location after clock transition.

full adder

The four-function full adder is controllable from select inputs S1 and S2 to perform:

A or B incrementation, or decrementation of B

Unconditional jumps or relative offsets

No change

Return to zero or one

Incrementation can be implemented by forcing a carry (high) into the ALU. In this mode either of the following options are possible:

1. Increment (A plus zero plus carry)
2. Increment B (zero plus B plus carry), or decrement B (all highs at A then A plus B with carry input low and disregard, don't use, carry out)
3. Increment the jump or offset (A plus B plus carry)

full adder (continued)

4. Start at zero or one and increment on each clock (select zero plus zero plus carry, then select zero plus B plus carry), or set register to N and decrement B (see 2 above).
5. No change (carry input is always active and removal of carry combined with either the ALU or register hold mode will retain the current address).

Unconditional jumps can be implemented by applying and selecting the jump directly from the data inputs to the output register. Offset can be accomplished by summing the output register with the offset magnitude (A plus B) with carry low.

The ALU functions are shown in Table IV.

TABLE IV. ADDRESS CONTROL FUNCTIONS

INPUTS		INTERNAL
S1	S2	Σi
H	H	0 PLUS 0 PLUS C-in
H	L	0 PLUS Bi PLUS C-in
L	H	Ai PLUS 0 PLUS C-in
L	L	Ai PLUS Bi PLUS C-in

compound generator functions

As the function-select lines of the register sources, push-pop stack, and adder are independent, compound functions can be selected to occur on the next clock transition.

Subroutine branches and returns can be simplified by saving the return or link addresses in the push-pop stack. This branch-and-save function can be accomplished on the same clock time as follows:

DATA-IN	ADDER	PUSH-POP STACK	REGISTER SOURCE
Branch address	Zero plus B plus one (S1 = H, S2 = L)	Push (S3 = S4 = H)	Data-in (S5 = S6 = L)

Up to four branches can be made with the return stored in the 4-word push-pop stack.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S482 . . . . . −55°C to 125°C
SN74S482 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. All voltage values are with respect to network ground terminal.

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